

M5275 Evaluation Board Errata

by: Microcontroller Division

This document identifies implementation differences between the M5275EVB and M5275EVBE and the description contained in the M5275EVB User's Manual. Check <http://www.freescale.com> for the latest updates.

This document applies to all revisions of the M5275EVB and M5275EVBE.

Contents

1	ASRAM	2
1.1	Description of Problem	2
1.2	Solution	2

1 ASRAM

1.1 Description of Problem

The EVB has a footprint for one 256 Kbytes × 16 asynchronous SRAM devices (Cypress Semiconductor – CY7C1041CV3310ZC). This memory device (U1) may be populated for benchmarking purposes. However, the EVBs have incorrectly interfaced to the ASRAM where addressing to (U1) is mapped [A0:A17] to the MCF5275's (U6) buffered address signals [B_A2:B_A19]. This is shown in Figure 1.

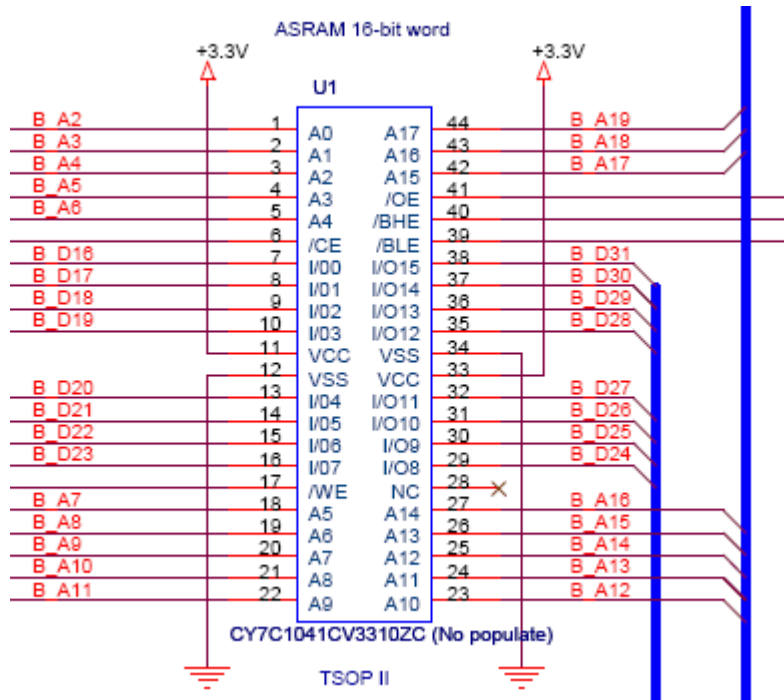


Figure 1. Example of Incorrect ASRAM Interface Found on EVBs

1.2 Solution

The EVBs should be interfaced to the ASRAM where addressing to (U1) is mapped [A0:A17] to the MCF5275's (U6) buffered address signals [B_A1:B_A18]. This is shown below in Figure 2.

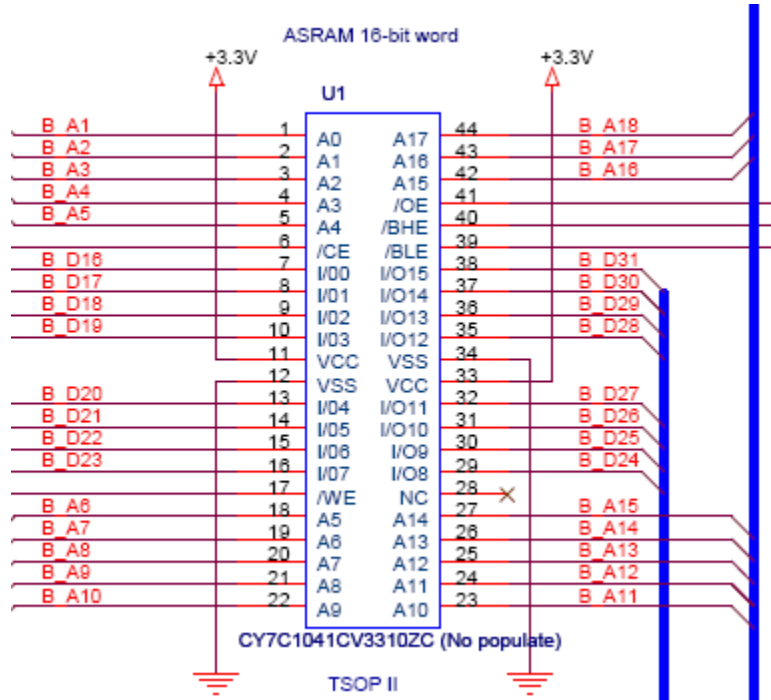


Figure 2. Example of Correct ASRAM Interface Found on EVBs.

The corrected addressing implementation is on the next revision of the evaluation board, M5275EVBE Rev. B.

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