

# Supplementary Information Regarding Brief Pulse Erratum on SG/SH I/O Pins during Power-On-Reset

## 1 Abstract

The 1M07J and 2M84G (and earlier) mask sets of the SG/SH32 and SG/SH8, respectively, have an erratum concerning a brief pulse on I/O pins while the MCU is being powered up. The pulse magnitude and duration are dependent on the power supply rise time. This Engineering Bulletin gives examples of the disturbance and offers suggestions for systems that may be affected by the behavior.

## 2 Description

This engineering bulletin provides additional information regarding the erratum for members of the SG32, SH32, SG8, and SH8 microcontroller (MCU) families. The erratum states “During a power-on-reset, a brief pulse occurs on I/O pins. The brief pulse, which is due to the gating of the integrated pullup resistors, may be able to drive active-high output circuits (for example,

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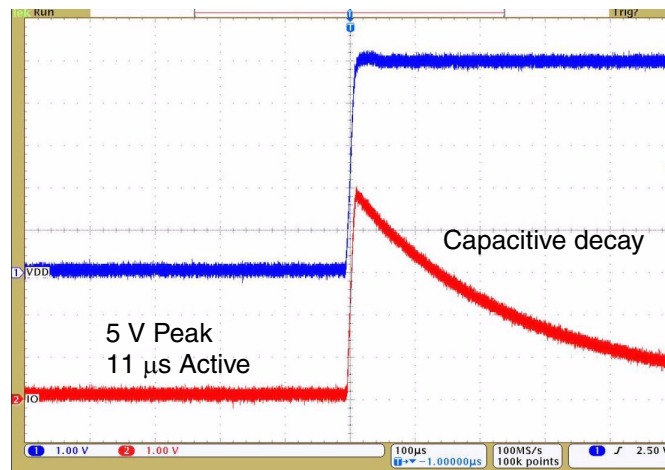
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## Description

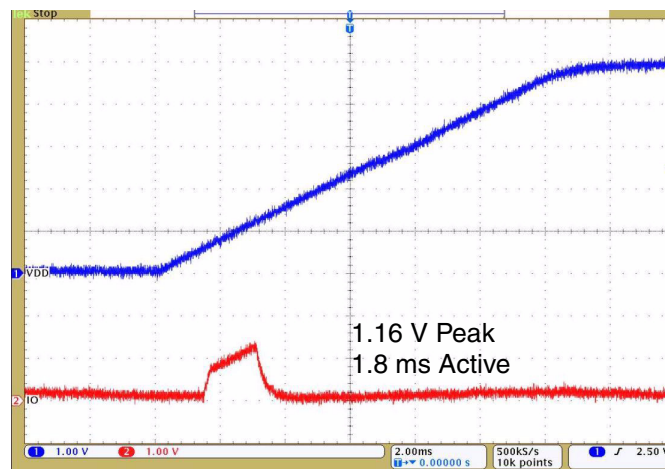
relay drivers or NPN transistors) momentarily. Input circuits are not affected.”

The integrated pullup resistor on each I/O pin is a weak p-channel MOSFET that is enabled by user software, typically for input pin biasing in an application. During powerup, the pullup is supposed to be disabled, as the port pin is intended to be high impedance. On the mask sets listed above, the pullup is provisionally enabled during the supply ramp until the pin POR logic becomes active. That is, the pullup is not intentionally enabled, and its behavior is dependent on power supply startup characteristics.

In general, with this erratum faster power supply rise times result in higher pulse amplitudes. [Figure 1](#) shows an I/O pin response during a relatively fast device power-up. [Figure 2](#) shows the response for a much slower power supply ramp. Note that the amplitude of the fast supply is much greater compared to that of the slower supply. Also note the relative duration of the inadvertent pulse – shorter for the fast rise time and longer for the slow rise time.



**Figure 1. 10 µs  $V_{DD}$  Ramp, No Load**



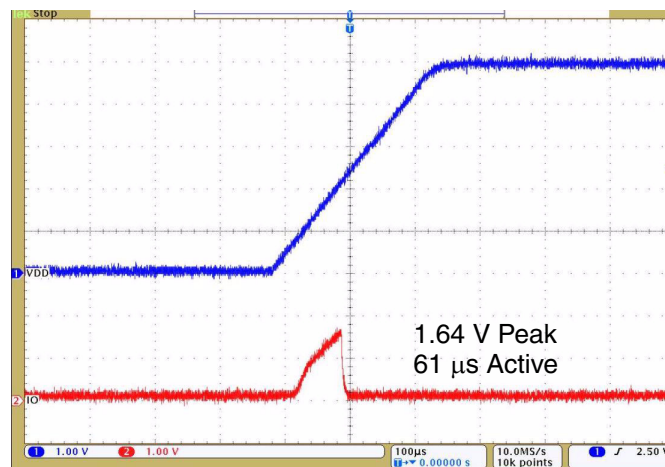
**Figure 2. 10 ms  $V_{DD}$  Ramp, No Load**

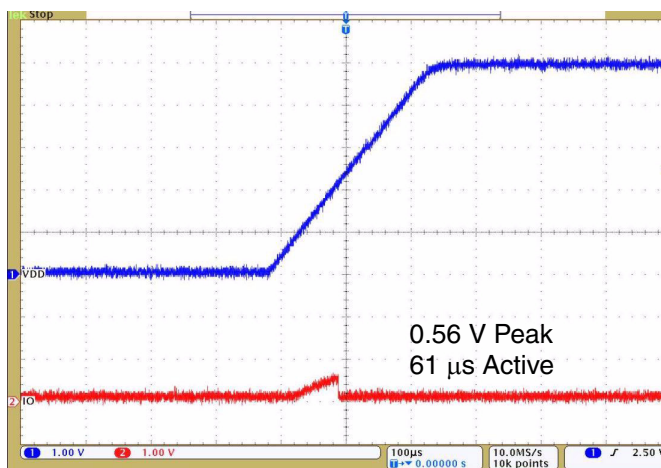
While Freescale cannot provide a mathematical relationship for the responses, we did characterize units to establish the trends. The data shown in [Table 1](#) can be used to determine an appropriate filter to attenuate the pulse(s) in an application if necessary.

**Table 1. Peak Voltage and Pulse Active Time vs  $V_{DD}$  Ramp Time**

$V_{DD}$ Ramp Time	No Load		100 k $\Omega$ Load		10 k $\Omega$ Load	
	Peak Voltage (V)	Pulse Active ( $\mu$ s)	Peak Voltage (V)	Pulse Active ( $\mu$ s)	Peak Voltage (V)	Pulse Active ( $\mu$ s)
10 $\mu$ s	5.00	11	3.79	15	1.23	15
50 $\mu$ s	3.42	28	2.54	27	0.85	27
100 $\mu$ s	2.74	43	2.01	40	0.67	40
200 $\mu$ s	2.26	66	1.64	61	0.56	61
500 $\mu$ s	1.90	128	1.38	114	0.47	114
1 ms	1.70	225	1.23	196	0.44	196
10 ms	1.16	1800	0.77	1340	0.18	1000

Note the trend with and without loads on the output pins. [Figure 3](#) shows the 200  $\mu$ s  $V_{DD}$  ramp time with a 100 k $\Omega$  load, while [Figure 4](#) shows the same ramp time with a 10 k $\Omega$  load. Practically, the no load measurements are not very applicable because most active high outputs will have loads.


**Figure 3. 200  $\mu$ s  $V_{DD}$  Ramp, 100 k $\Omega$  Load**



**Figure 4. 200  $\mu$ s  $V_{DD}$  Ramp, 10 k $\Omega$  Load**

The two main items to consider are output pin usage and power supply ramp time. Critical active high circuits, like relay or TRIAC drivers, that are driven by output pins are the primary concern. In general, these outputs have external pull-down resistors to provide a safe power-up transition. A small capacitor may be the appropriate filter element if the equivalent resistance of the driver network is relatively small (<10 k $\Omega$ ). An additional RC filter may be required if the impedance of the driver network is relatively high (>10 k $\Omega$ ).

Power supply ramp times are dependent on many factors, including input voltage and supply loading. While the scope traces in [Figure 1](#) through [Figure 4](#) show idealized linear rise times (since a pulse generator was used to control the ramps), most system power supplies exhibit traditional capacitive rise times. Power supply rise times are not generally specified in regulator data sheets, so this determination must be made empirically by measuring the ramp in the actual system. A suggestion for a practical range of ramp times would be to allow an order of magnitude above and below the measured time. For instance, a measured rise time of 5 ms would suggest a practical range of 0.5 ms to 50 ms.

What kind of output circuits do not need these precautions? Low frequency indicators like LEDs are not the concern. Likewise, signals that are connected to other logic devices, like serial chips, do not respond to pulses of this duration as the logic chips are powering up as well during this time.

Another aspect that may need consideration is unused pins. Unused or unbonded pins should be terminated by configuring these I/O pins as inputs with pullups enabled, or as outputs driving high or low. Freescale recommends that user software configures the unused and unbonded pins as outputs driving low. In this configuration unused pins are left unconnected on the circuit board.

### 3 Summary

The workaround for the SG/SH erratum is only needed under certain system conditions – critical active-high output pin, fast power supply rise time, and high impedance loading. Otherwise, the erratum workaround will not be a practical system concern.



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