The MSC8157 and MSC8158 family DSPs are members of the Freescale family of high-end multicore programmable digital signal processors (DSPs). They both use the fourth-generation SC3850 core.

This engineering bulletin discusses the differences between the DSP core subsystems and the peripheral blocks used in the DSP devices. Unless otherwise noted, MSC8157 includes the following devices:

- MSC8157
- MSC8157E

MSC8158 includes the following devices:

- MSC8158
- MSC8158E
# Summary of Differences

Table 1 summarizes the differences between the device families; identical functionality is not listed. Figure 1 and Figure 2 show block diagrams of the MSC8157 and MSC8158 device families, respectively.

<table>
<thead>
<tr>
<th>Feature</th>
<th>MSC8157</th>
<th>MSC8178E</th>
<th>MSC8158</th>
<th>MSC8188E</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset</td>
<td>– RCW modified to support 10-lane SerDes interface with device-specific multiplexing.</td>
<td>– RCW modified to support 8-lane SerDes interface with device-specific multiplexing.</td>
<td>– None</td>
<td>– Supports SEC 3.1.0</td>
</tr>
<tr>
<td>Security Engine Controller (SEC)</td>
<td>– None</td>
<td>– Supports SEC 3.1.0</td>
<td>– None</td>
<td>– Supports SEC 3.1.0</td>
</tr>
<tr>
<td>High Speed Serial Interface (HSSI)</td>
<td>– Supports two Serial RapidIO controllers, one enhanced messaging unit (eMSG), two DMA units, two DMA to OCN bridges, PCI Express controller, 6 CPRI controllers, and 10 SerDes lanes.</td>
<td>– Supports two Serial RapidIO controller, one enhanced messaging unit (eMSG), two DMA units, two DMA to OCN bridges, 6 CPRI controllers, and 6 SerDes lanes.</td>
<td>– Supports two Serial RapidIO controller, one enhanced messaging unit (eMSG), two DMA units, two DMA to OCN bridges, 6 CPRI controllers, and 6 SerDes lanes.</td>
<td>– Supports two Serial RapidIO controller, one enhanced messaging unit (eMSG), two DMA units, two DMA to OCN bridges, 6 CPRI controllers, and 6 SerDes lanes.</td>
</tr>
<tr>
<td></td>
<td>– 10-lane SerDes port multiplexing two x1/x2/x4 Serial RapidIO ports, one x4/x2/x1 PCI Express port, up to 6 CPRI lanes, and two SGMII interfaces (controlled by the QUICC Engine subsystem).</td>
<td>– 8-lane SerDes port multiplexing one x1/x2/x4 Serial RapidIO port, one x1/x2 Serial RapidIO port, up to 6 CPRI lanes, and two SGMII interfaces (controlled by the QUICC Engine subsystem).</td>
<td>– Supports transfer rates up to 5 GHz for Serial RapidIO and PCI Express and up to 6.144 Gbaud for CPRI.</td>
<td>– Supports transfer rates up to 5 GHz for Serial RapidIO and up to 6.144 Gbaud for CPRI.</td>
</tr>
<tr>
<td>Serial RapidIO Controller</td>
<td>– Two serial RapidIO ports with one eMSG</td>
<td>– One serial RapidIO port with one eMSG</td>
<td>– One serial RapidIO port with one eMSG</td>
<td>– One port at x1, x2, or x4 up to 5 Gbaud</td>
</tr>
<tr>
<td></td>
<td>– x1, x2, or x4 up to 5 Gbaud</td>
<td>– x1, x2, or x4 up to 5 Gbaud</td>
<td>– x1, x2, or x4 up to 5 Gbaud</td>
<td>– Not supported.</td>
</tr>
<tr>
<td></td>
<td>– Pass-through between the two ports.</td>
<td>– Pass-through between the two ports.</td>
<td>– Pass-through between the two ports.</td>
<td>– Pass-through between the two ports.</td>
</tr>
<tr>
<td>PCI Express</td>
<td>– Designed to comply with PCI Express Base Specification, Revision 2.0.</td>
<td>– Designed to comply with PCI Express Base Specification, Revision 2.0.</td>
<td>– Enhanced Turbo and Viterbi Processing Element (eTVPE)</td>
<td>– Not supported.</td>
</tr>
<tr>
<td></td>
<td>– x1, x2, or x4 up to 5 Gbaud</td>
<td>– x1, x2, or x4 up to 5 Gbaud</td>
<td>– Downlink Encoding Processing Element (DEPE)</td>
<td>– Not supported.</td>
</tr>
<tr>
<td>MAPLE-B2</td>
<td>– Enhanced Turbo and Viterbi Processing Element (eTVPE)</td>
<td>– Enhanced Turbo and Viterbi Processing Element (eTVPE)</td>
<td>– Enhanced Turbo and Viterbi Processing Element (eTVPE)</td>
<td>– Enhanced Turbo and Viterbi Processing Element (eTVPE)</td>
</tr>
<tr>
<td></td>
<td>– Downlink Encoding Processing Element (DEPE)</td>
<td>– Downlink Encoding Processing Element (DEPE)</td>
<td>– Downlink Encoding Processing Element (DEPE)</td>
<td>– Downlink Encoding Processing Element (DEPE)</td>
</tr>
<tr>
<td></td>
<td>– Equalization Processing Element (EQPE)</td>
<td>– Equalization Processing Element (EQPE)</td>
<td>– Equalization Processing Element (EQPE)</td>
<td>– Equalization Processing Element (EQPE)</td>
</tr>
<tr>
<td></td>
<td>– Three Fourier Transform Processing Elements (eFTPEs)</td>
<td>– Three Fourier Transform Processing Elements (eFTPEs)</td>
<td>– Three Fourier Transform Processing Elements (eFTPEs)</td>
<td>– Three Fourier Transform Processing Elements (eFTPEs)</td>
</tr>
<tr>
<td></td>
<td>– Chip Rate Processing Element (CRPE)</td>
<td>– Chip Rate Processing Element (CRPE)</td>
<td>– Chip Rate Processing Element (CRPE)</td>
<td>– Chip Rate Processing Element (CRPE)</td>
</tr>
<tr>
<td></td>
<td>– Cyclic Redundancy Check Processing Element (CRCPE)</td>
<td>– Cyclic Redundancy Check Processing Element (CRCPE)</td>
<td>– Cyclic Redundancy Check Processing Element (CRCPE)</td>
<td>– Cyclic Redundancy Check Processing Element (CRCPE)</td>
</tr>
<tr>
<td>Device IDs</td>
<td>– RapidIO DIDCAR[DI] = 0x1828</td>
<td>– RapidIO DIDCAR[DI] = 0x18A</td>
<td>– RapidIO DIDCAR[DI] = 0x181C</td>
<td>– RapidIO DIDCAR[DI] = 0x181E</td>
</tr>
<tr>
<td></td>
<td>– PCI Express Device ID = 0x1828</td>
<td>– PCI Express Device ID = 0x182a</td>
<td>– PCI Express Device ID = 0x181C</td>
<td>– PCI Express Device ID = Not supported</td>
</tr>
<tr>
<td></td>
<td>– JTAG ID Register = 0x0188401D</td>
<td>– JTAG ID Register = 0x0188401D</td>
<td>– JTAG ID Register = 0x0188401D</td>
<td>– JTAG ID Register = Not supported</td>
</tr>
<tr>
<td></td>
<td>– SPRIDR[PARTID] = 0x8305</td>
<td>– SPRIDR[PARTID] = 0x830D</td>
<td>– SPRIDR[PARTID] = 0x8303</td>
<td>– SPRIDR[PARTID] = 0x8300B</td>
</tr>
<tr>
<td>Package/Pinout</td>
<td>– Designed to accommodate the updated functionality.</td>
<td>– Supports 10 differential SerDes lanes (A through J)</td>
<td>– Designed to accommodate the updated functionality.</td>
<td>– Supports 8 differential SerDes lanes (C through J)</td>
</tr>
<tr>
<td></td>
<td>– Supports 10 differential SerDes lanes (A through J)</td>
<td>– Otherwise, pin-compatible with MSC8158/E.</td>
<td>– Otherwise, pin-compatible with MSC8158/E.</td>
<td>– Otherwise, pin-compatible with MSC8157/E.</td>
</tr>
</tbody>
</table>
Differences Between the MSC8157 and the MSC8158 DSPs, Rev. 1

Summary of Differences

**Figure 1. MSC8157 Block Diagram**

- JTAG IEEE 1149.6
- DDR Controller
- M3 Memory 3072 Kbyte
- MAPLE-B2
- SEC (opt)
- DMA 32 ch

**CLASS**

- SC3850 DSP Core
- Six DSP Cores at 1 GHz
- Two RMII SPI
- Note: The arrow direction indicates master or slave.

**Additional Modules**

- Boot ROM
- I2C
- Virtual Interrupts
- SEC (opt)
- MAPLE-B2

**Additional Features**

- DDR Interface 64/32-bit 1333 MHz data rate
- UART
- Clocks
- Timers
- Reset
- Semaphores
- Virtual Interrupts
- Boot ROM
- SPI
- Two SGMII
- Two SGMII

**Figure 2. MSC8158 Block Diagram**

- JTAG IEEE 1149.6
- DDR Controller
- M3 Memory 3072 Kbyte
- MAPLE-B2
- SEC (opt)
- DMA 32 ch

**CLASS**

- SC3850 DSP Core
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**Additional Modules**

- Boot ROM
- I2C
- Virtual Interrupts
- SEC (opt)
- MAPLE-B2

**Additional Features**

- DDR Interface 64/32-bit 1333 MHz data rate
- UART
- Clocks
- Timers
- Reset
- Semaphores
- SPI
- Two SGMII
- Two SGMII

Two Serial RapidIO x1/x2/x4 up to 5 Gbaud
- Six lanes CPRI v4.1 up to 6.144 Gbaud
- PCI-Express x1/x2/x4 up to 5 Gbaud
- Two SGMII
2  Reset

The reset configuration word (RCW) in the MSC8157 is different from the MSC8158 to support multiplexing for the different interface devices. The 10-lane SerDes interface on the MSC8157 uses A through J. The 8-lane interface on the MSC8158 uses lanes C through J. The configuration values for the common interfaces are identical. The configuration values for the PCI Express and the second RapidIO port that are supported by the MSC8157 are not valid on the MSC8158.

3  Security Engine (SEC)

The optional SEC block is available on both the MSC8157E and MSC8158E devices. The SEC supports version 3.1.0 technology which includes the SNOW algorithm that is essential for 3G-LTE applications.

4  High Speed Serial Interface (HSSI)

The MSC8157 and MSC8158 HSSI modules use an internal frequency of 500 MHz and a 1.5 V for the differential I/O interface; therefore, you can use the nominal 1.5 V input used for the DDR3 memory for the differential data lines as the power source. Connect the power supply to SXPVDD using a filter to suppress noise. The SRIO_IMP_CAL_RX signal should be connected to SXCVDD through a 200 Ω resistor. The SRIO_IMP_CAL_TX signal should be connected to SXPVDD through a 200 Ω resistor.

The MSC8157 family HSSI subsystem supports two Serial RapidIO ports, six Common Public Radio Interface (CPRI) controllers, one PCI Express controller, one enhanced messaging unit (eMSG) that supports advanced message classification and queueing, two dedicated DMA controllers, two DMA-to-OCN bridges, a CLASS1 module to interface to the internal memory buses, and a 10-lane SerDes port shared by the RapidIO ports, CPRI ports, PCI Express ports, and the two SGMII ports. The device allows selection of either or both RapidIO interfaces in x4, x2, or x1 mode at up to 5 Gbaud, a PCI Express interface in x4, x2, or x1 mode at 2.5 or 5 Gbaud, up to 6 CPRI lanes with transfer rates up to 6.144 Gbaud, and up to two SGMII interfaces in x1 mode.

The MSC8158 family HSSI subsystem supports two Serial RapidIO ports (1 = x1/x2/x4; 2 = x1/x2), six Common Public Radio Interface (CPRI) controllers, one enhanced messaging unit (eMSG) that supports advanced message classification and queueing, two dedicated DMA controllers, two DMA-to-OCN bridges, a CLASS1 module to interface to the internal memory buses, and an 8-lane SerDes port shared by the RapidIO ports, CPRI ports, and the two SGMII ports. The device allows selection of two RapidIO interfaces (1 in x4, x2, or x1 mode; 2 in x2 or x1 mode) at up to 5 Gbaud, up to 6 CPRI lanes with transfer rates up to 6.144 Gbaud, and up to two SGMII interfaces in x1 mode.

Table 2 summarizes the differences for easy reference.

<table>
<thead>
<tr>
<th>Function</th>
<th>MSC8157</th>
<th>MSC8158</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>nominal 1.5 V</td>
<td>nominal 1.5 V</td>
</tr>
<tr>
<td>Internal Frequency</td>
<td>500 MHz</td>
<td>500 MHz</td>
</tr>
<tr>
<td>SerDes lanes</td>
<td>10</td>
<td>8</td>
</tr>
<tr>
<td>SGMII</td>
<td>Two interfaces at 2.5 Gbaud</td>
<td>Two interfaces at 2.5 Gbaud</td>
</tr>
</tbody>
</table>

Table 2: SerDes Functional Differences Between MSC8157 and MSC8158
The MSC8157 supports two Serial RapidIO ports and one eMSG within the HSSI and supports RapidIO Interconnect Specification Revision 2.1. The HSSI ports support x1/x2/x4 RapidIO operation up to 5 Gbaud. The HSSI includes pass-through support between the two RapidIO ports to eliminate the need for an on-board serial RapidIO switch. In addition, the controllers provide expanded RapidIO protocol support.

The MSC8158 includes two Serial RapidIO ports and one eMSG within the HSSI and supports RapidIO Interconnect Specification Revision 2.1. The HSSI port supports x1/x2/x4 RapidIO operation for one interface and x1/x2 RapidIO operation for the second interface up to 5 Gbaud. In addition, the controller provides expanded RapidIO protocol support.

The MSC8157 family MAPLE-B2 subsystem supports the following Processing Elements (PEs):

- Enhanced Turbo and Viterbi Processing Element (eTVPE)
- Downlink Encoding Processing Element (DEPE)
- Equalization Processing Element (EQPE)
- Three Fourier Transform Processing Elements (eFTPEs)
- Chip Rate Processing Element (CRPE)
- Cyclic Redundancy Check Processing Element (CRCPE)

This allows the MSC8157 device to support the following:

- Turbo decoding including rate matching for 3GLTE, UMTS, and WiMAX
- Turbo encoding: information bits encoding including rate matching for 3GLTE, WiMAX, and UMTS.
- Viterbi decoding

### Table 2. SerDes Functional Differences Between MSC8157 and MSC8158

<table>
<thead>
<tr>
<th>Function</th>
<th>MSC8157</th>
<th>MSC8158</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI Express</td>
<td>Single (Rev. 2.0) x1/x2/x4 at 2.5 or 5.0 Gbaud</td>
<td>Not supported</td>
</tr>
<tr>
<td>CPRI</td>
<td>Up to 6 lanes at 1.2288, 2.4576, 3.072, 4.9152, or 6.144 Gbaud with daisy-chain capability for cascading devices</td>
<td>Up to 6 lanes at 1.2288, 2.4576, 3.072, 4.9152, or 6.144 Gbaud with daisy-chain capability for cascading devices</td>
</tr>
<tr>
<td>Serial RapidIO</td>
<td>Two interfaces x1/x2/x4 at 1.25/2.5/3.125/5 Gbaud</td>
<td>Interface 1 x1/x2/x4 at 1.25/2.5/3.125/5 Gbaud Interface 2 x1/x2 at 1.25/2.5/3.125 Gbaud</td>
</tr>
</tbody>
</table>
The MSC8158 family MAPLE-B2 subsystem supports the following Processing Elements (PEs):

- Enhanced Turbo and Viterbi Processing Element (eTVPE)
- Downlink Encoding Processing Element (DEPE)
- Three Fourier Transform Processing Elements (eFTPEs)
- Chip Rate Processing Element (CRPE)
- Cyclic Redundancy Check Processing Element (CRCPE)

This allows the MSC8158 devices to support the following:

- Turbo decoding including rate matching
- Turbo encoding: information bits encoding including UMTS.
- Viterbi decoding
- FFT/iFFT processing.
- DFT/iDFT processing.
- CRC check and insertion
- UMTS downlink spreading, scrambling, gain and combining of Physical Channels including STTD, TSTD and Closed Loop Mode 1 operation per channel. Chip rate despreading/spreading and descrambling/scrambling.
- UMTS uplink low latency DCPCCH and E-DPCCH interpolation, despreading, descrambling.
- UMTS Path searcher and RACH correlations in frequency domain.

Differences Between the MSC8157 and the MSC8158 DSPs, Rev. 1

Freescale Semiconductor
8 Device IDs

Table 3 summarizes the Device IDs for the MSC8157 and MSC8158 devices.

<table>
<thead>
<tr>
<th>Device ID</th>
<th>MSC8157</th>
<th>MSC8157E</th>
<th>MSC8158</th>
<th>MSC8158E</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPRIDR[PARTID]</td>
<td>0x8305</td>
<td>0x830D</td>
<td>0x8303</td>
<td>0x830B</td>
</tr>
<tr>
<td>RapidIO DIDCAR[DI]</td>
<td>0x1828</td>
<td>0x182A</td>
<td>0x181C</td>
<td>0x181E</td>
</tr>
<tr>
<td>PCI Express Device ID</td>
<td>0x1828</td>
<td>0x182A</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>JTAG ID Register</td>
<td>0x0188401D</td>
<td>0x0188401D</td>
<td>0x0188401D</td>
<td>0x0188401D</td>
</tr>
</tbody>
</table>

9 Package/Pinout Differences

The MSC8157/MSC8157E and MSC8158/MSC8158E DSPs use the same device package with the pinout modified to reflect device functionality. Table 4 shows the differences between the MSC8157/MSC8157E and MSC8158/MSC8158E pinouts; the table does not include pinouts that are not changed.

<table>
<thead>
<tr>
<th>Ball Number</th>
<th>Signal Name</th>
<th>MSC8157/MSC8157E</th>
<th>MSC8158/MSC8158E</th>
</tr>
</thead>
<tbody>
<tr>
<td>M23</td>
<td>SD_A_TX</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>M24</td>
<td>SD_A_TX</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>M27</td>
<td>SD_A_RX</td>
<td>SXCVSS (not a ground pin)</td>
<td></td>
</tr>
<tr>
<td>M28</td>
<td>SD_A_RX</td>
<td>SXCVSS (not a ground pin)</td>
<td></td>
</tr>
<tr>
<td>N25</td>
<td>SD_B_TX</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>N26</td>
<td>SD_B_TX</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>P27</td>
<td>SD_B_RX</td>
<td>SXCVSS (not a ground pin)</td>
<td></td>
</tr>
<tr>
<td>P28</td>
<td>SD_B_RX</td>
<td>SXCVSS (not a ground pin)</td>
<td></td>
</tr>
</tbody>
</table>