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MPC5746C STCU BIST Configuration

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Contents

1 Introduction

This document describes the MPC5746C default Self-Test Control Unit (STCU) configuration for offline Built-In Self-Test (BIST). The default STCU configuration is programmed in the MPC5746C UTEST FLASH section during factory test and enables BIST execution at device startup events, as specified in the MPC5746C Reference Manual. Also included in this document are details on the default configuration settings for BIST faults and recommendations on handling BIST faults.

2 STCU BIST Configuration Summary

- BIST enabled by default
- Overall coverage level: ASIL-B
- FMPLL: 40 MHz
- LBIST: Not available for MPC5746C
- MBIST:
  - Memory partitions 0-44, parallel and sequential execution phases (see Table 2)
  - Coverage/Algorithm: Auto Test Mode (18N)
  - Execution time: 6.2 ms

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3 BIST Execution

BIST will execute at the following start-up events:

- Power-on reset (POR)
- Long functional external reset
- Destructive reset

4 BIST Clock Settings

STCU offline BIST uses the PLL and IRC clock to generate an internal 40 MHz clock. No external clocks are required to run offline self-test.

5 MBIST

MBIST is executed for each of the memories listed in Table 1. The memories are segmented into 45 individual memory partitions as shown in Table 1.

The default MBIST configuration for the MPC5746C executes Auto Test Mode (18N), which provides less than 90% coverage.

Table 1. MBIST partitions

Partition number	Memory association
0	PRAM0
1	
2	
3	
4	
5	PRAM1
6	
7	Z4 ICACHE
8	
9	
10	
11	Z4 ITAG
12	Z4 DCACHE
13	
14	
15	
16	Z4 DTAG
17	HSM RAM

Table continues on the next page...

Table 1. MBIST partitions (continued)

18	
19	
20	
21	HSM DCACHE
22	
23	HSM TAG
24	
25	FLEXCAN
26	
27	
28	
29	
30	
31	
32	
33	FLEXRAY DATA
34	DMA RAM
35	FLEXRAY LUTO
36	ENET RX FIFO
37	FLEXRAY ROM
38	BAR ROM
39	FLEXRAY LUT1
40	ENET TX FIFO
41	ENET RXPARSER
42	
43	PRAM1
44	

The default execution order of the MBIST partitions is illustrated in the table below. Note that MBIST tests are executed in parallel and sequential phases, to provide an optimal balance of execution time and current consumption.

Table 2. MBIST execution order

Phase 1	**Phase 2**
System RAM (1-6, 43, 44) HSM (17)	Remaining partitions (0, 7-16, 18-42)

6 Disable BIST Execution

The default BIST configuration for MPC5746C enables BIST to automatically execute after certain start-up and reset events as described in BIST Execution. If desired, BIST execution may be disabled.

To disable BIST, a single Device Configuration Format (DCF) record should be written to the UTEST FLASH section immediately after the last valid DCF entry in the UTEST, as shown in the figure below. The DCF record area starts at 0x00400300. After the DCF record area, the first address which contains 0xFFFFFFFF_FFFFFFFF is the first open UTEST memory address.

The following DCF record should be written to the first open UTEST memory address to disable BIST:

0x7F000000, 0x0008000C

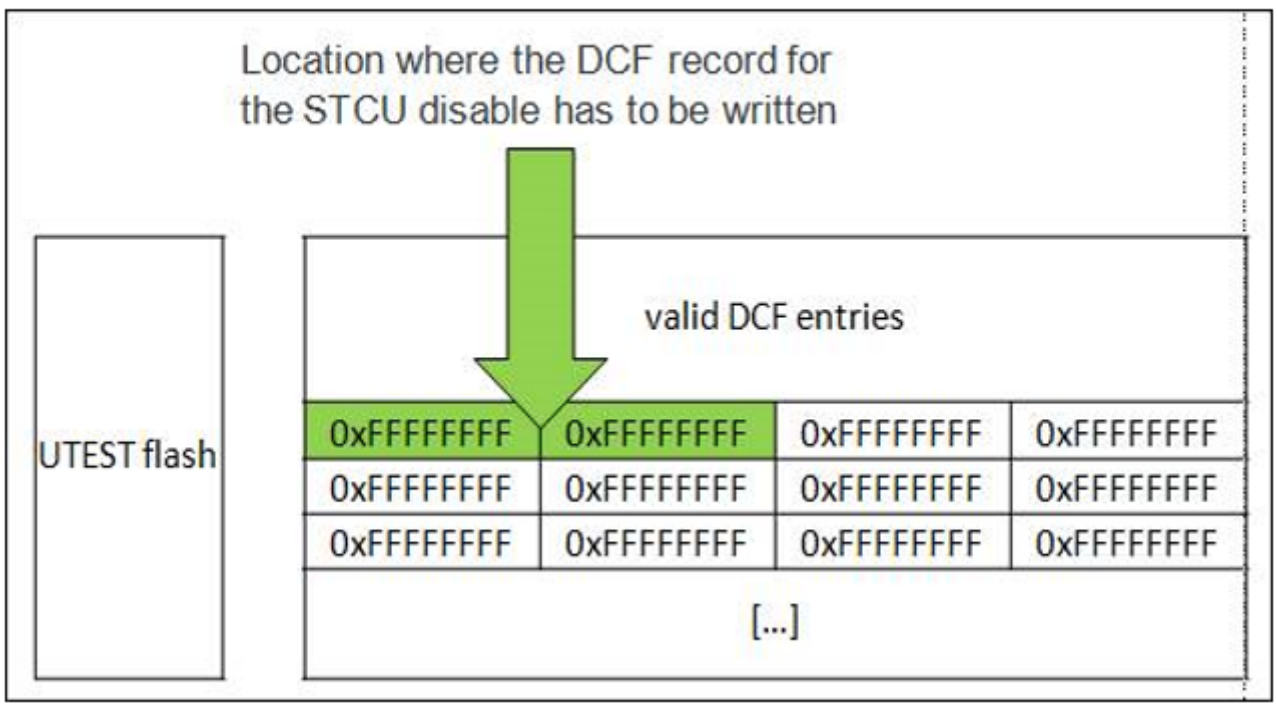

Figure 1. Open UTEST memory location

It should be confirmed that BIST is properly disabled, by verifying that the values of all of the following registers are all zeros:

- STCU2 Error Register: STCU2_ERR_STAT
- STCU2 Off-line MBIST Status Low Register: STCU2_MBSL
- STCU2 Off-line MBIST Status Medium Register: STCU2_MBSM
- STCU2 Off-line MBIST End Flag Low Register: STCU2_MBEL
- STCU2 Off-line MBIST End Flag Medium Register: STCU2_MBEM

7 Fault Handling

The default configuration for the MPC5746C sets all BIST faults as recoverable faults.

After BIST execution, application software should check the following registers to determine whether a fault has occurred:

- STCU2 error register: STCU2_ERR_STAT (will read all zeros if no fault occurred)
- Recoverable Faults Status Flag: STCU2_ERR_STAT[RSF]

If a fault has occurred, the following STCU2 status registers should be read to determine the source of the fault:

- STCU2 Off-Line MIBST Status Low Register: STCU2_MBSL (expected value 0xFFFF_FFFF)
- STCU2 Off-Line MBIST Status Medium Register: STCU2_MBSM (expected value 0x0000_1FFF)

If a fault does occur, application software should check the FCCU Status register to see if a multi-bit error has occurred. Since single bit errors are correctible via ECC, a single bit error should not be considered a fatal error.

Please consult the MPC5746C Reference Manual and Safety Manual to ensure that fault handling is performed correctly in order to achieve required safety coverage levels.

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