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Power Management on the MC68307

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Introduction

The fully static Integrated Multiple-Bus Processor (IMBP), the MC68307, has a number of flexible power management features that enable the power consumption to be minimised for different applications. This engineering bulletin describes how to use these features to best effect in reducing overall system power consumption and also gives actual current measurements that were made on a development system to illustrate the benefits of these techniques.

The values for IDD given in the tables are typical values at room temperature measured in the lab for an IMBP in a typical application and include the current due to I/O loads. These current figures should not be compared with data book values which exclude the effects of I/O currents.

Fully static operation

The IMBP is fully static; this means that the clock to the device can be stopped completely without causing damage, in addition the clock can be restarted with no loss of status occurring.

These two fundamental benefits of fully static operation are utilised in the IMBP power management features. The IMBP allows the clocks to different modules within the device to be stopped under software control in order to minimise power consumption for a particular user application. The external clock input can also be varied in frequency between DC (i.e. stopped externally) and the maximum operating frequency (16.67 MHz).

By setting the appropriate bits in the configuration register the internal clocks to the MBus, Timer, UART, CLKOUT and CPU can be individually stopped. With the exception of the CPU these clocks can all be restarted by clearing the corresponding bit in the configuration register. When a module clock is turned off the module current consumption is reduced to very low leakage levels.

Table 1 gives typical percentage power savings that can be made by stopping the clocks to modules that are not used in a particular operating mode. These figures are from measurements taken on a development board. They represent percentages of full operating power consumption and are averages over four different test cases (16.67MHz and 8MHz at 5V and 3.3V).

Table 1 Power Contribution from Modules

Module	Percentage IDD
All Operational	100%
CLKOUT	4%
MBus	5%
Timer	6%
UART	21%
CPU (68000)	59%
Low-Power Standby	5%

Prescalable CPU clock

It is apparent from Table 1 that the 68EC000 CPU core contributes the most significant percentage of the total power consumption. As well as being able to stop the clock to the CPU completely (when the CPU clock is stopped it cannot process code) this clock can be selectively programmed to a prescaled value. This is achieved by writing to the LPEN bit in the configuration register with the LPCD bits set to select the required prescale value.

Only the CPU clock is divided by this prescale value, the enabled clocks to the peripheral modules remain at the system clock frequency. Hence the module interfaces will operate as normal.

This mode of operation is useful when the CPU is required to do some background housekeeping tasks, which do not require the full processing power of the CPU, but one or more of the peripheral modules are required to be operating at full speed. The CPU can subsequently select full speed clock by writing to the configuration register when an event occurs that requires the full processing power.

The power consumption of the CPU is approximately proportional to the frequency, hence by carefully selecting the correct prescale value for the current task the power contribution of the CPU to the overall device can be minimised. An example of the effect of prescaling the CPU clock is given in Table 2, in this table all the other modules are getting clocked at EXTAL frequency.

Table 2 Effect of Prescaling CPU Clock

EXTAL Freq	CPU Freq	Vdd	IDD
16,67 MHz	16.67 MHz	5 V	46.2 mA
16,67 MHz	8.34 MHz (div 2)	5 V	34.8 mA
16.67 MHz	65.1 kHz (div 256)	5 V	19.9 mA
8.0 MHz	8.0 MHz	3.3 V	13.1 mA
8.0 MHz	4.0 MHz (div 2)	3.3 V	9.7 mA
8.0 MHz	31.2 kHz (div 256)	3.3 V	5.8 mA

Wake-up

When the CPU clock has been stopped it can only be restarted by a wake-up condition or a system reset. Any event that causes an interrupt will wake-up the CPU. For an interrupt to occur the corresponding module must be getting clocked and the interrupt priority level must be set to non-zero in the corresponding field of the interrupt control register.

It is also possible to set a bit in the configuration register that automatically restarts the clock to the UART when a falling edge is detected on the RXD line. Any subsequent interrupt from the UART module will wake-up the CPU.

This very flexible feature enables the CPU to wake-up in response to many different events, for example:-

- UART receives a character
- MBus activity is detected
- After a fixed time by programming a timer
- An external interrupt occurs

Because there is no loss of data in the fully static CPU core the wake-up latency is reduced to the minimum, only 10 system clocks. When the CPU wakes-up it immediately processes the interrupt and then returns to the main-line code from which it stopped its own clock.

All enabled interrupts will wake-up the CPU, if the interrupt mask in the CPU is set to a level greater than the active interrupt then this interrupt will not be processed immediately by the CPU. This technique gives the absolute minimum wake-up latency since time-critical code can be placed immediately after the instruction that stopped the CPU clock but before the interrupt mask is lowered to process the interrupt which caused the wake-up.

A STOP instruction is not required when the IMBP is put into Low-Power Standby mode, if such an instruction is used it will be handled correctly by the CPU. Care must be taken with the interrupt mask since any interrupt wakes-up the CPU but only interrupts of priority greater than the mask cause the CPU to exit stop mode. The wake-up latency is increased slightly to 24 system clocks when a STOP instruction is used.

The IMBP does not require or generate a reset on wake-up. If the IMBP is reset the CPU clock and all the other internal clocks are restarted, however the wake-up latency will be be large since reset exception processing is required.

Low-Power Standby Mode

When all the internal clocks are stopped, including the CPU, the IMBP is said to be in low-power standby mode.

In low-power standby mode the external clock, either crystal oscillator or square wave input, is still toggling. The only logic internal to the IMBP that is getting clocked is the reset circuit and interrupt controller. The device can wake-up from low-power standby mode by an external interrupt on $\overline{\text{IRQ7}}$ or any of the $\overline{\text{INTx}}$ inputs. In addition the UART clock can automatically restart when a falling edge is detected on RXD, and subsequently wake-up the CPU when an interrupt occurs.

The CPU is arbitrated off the system bus when it enters low-power standby mode. The address and data busses are tri-stated. For a system that has the IMBP in this mode for prolonged periods of time the system address and data busses should be fitted with high value (e.g. 50-100Kohms) pull-up resistors to prevent these busses floating to mid-range voltage levels and hence generating large currents in input

buffers.

When a crystal is connected across EXTAL and XTAL pins on the IMBP the contribution of the oscillator cell to the standby current is large. Depending on the type of crystal used this bias current can be up to several milliamps. Careful choice of crystal and board layout can help minimise the effect of the bias current, but it will always make a significant contribution to standby current. If an external oscillator is used to generate a square wave input to EXTAL the bias current is much less. When an external oscillator is used the XTAL pin should be left completely unconnected. (On our application development board 600uA were saved when the superfluous wire on XTAL was removed).

Low-power standby mode consumes about 4% to 6% of the fully operational power depending on the configuration of the oscillator pins.

The IDD current measured for Low-Power Standby mode is given in Table 3. This table also gives the value of IDD measured when all the IMBP clocks are operational and also the case when CPU is running but all other peripherals have their clocks switched off.

Table 3 Typical Idd Measurements

EXTAL Freq	Vdd	Whole chip on	CPU on Peripherals off	Low-Power Standby
16.67 MHz	5 V	46.2 mA	30.0 mA	3.2 mA
8.0 MHz	5 V	23.6 mA	15.3 mA	1.64 mA
1.0 MHz	5 V	2.95 mA	1.9 mA	260 uA
16.67 MHz	3.3 V	27.2 mA	17.7 mA	1.93 mA
8.0 MHz	3.3 V	13.1 mA	8.5 mA	970 uA
1.0 MHz	3.3 V	1.62 mA	1.05mA	140 uA

Low-Power Stop Mode

The power consumption of the IMBP can be minimised by stopping the clock to the EXTAL pin externally. This is referred to as Low-Power Stop mode. External hardware is required to control the system clock circuit. The current consumption of the IMBP is at an absolute minimum in this mode.

Note that since the external clock input to the IMBP is stopped the device cannot wake-up from Low-Power Stop mode directly.

Because the IMBP is fully static the clock can be stopped at any time and in any phase. Lowest power will be obtained if the clock is stopped after the device has been put into low-power standby mode. If the clock is stopped when the CPU is executing a bus cycle or processing an instruction the current will not be minimal, low-power standby mode uses arbitration to ensure that the CPU is idle before stopping the internal clock.

When the clock is restarted the IMBP will continue processing from where it was previously with no loss of status. If the device is in low-power standby mode an interrupt will be required to wake-up the CPU.

Instead of stopping the clock externally the frequency could be reduced to a very low value in order to

minimise power. The whole IMBP could operate at this reduced frequency, allowing timers for example to wake-up the CPU after a long delay and subsequently set a general purpose port line to reselect the maximal frequency external clock.

Whenever the external clock is being stopped, started or multiplexed care must be taken to ensure that no pulses narrower than the specified minimum clock high or low periods are generated (Minimum pulse width = 27 nS). If an external crystal is stopped then started again there may be considerable wake-up latency due to the crystal start-up time, this depends on the external component selection and is not a function of the IMBP.

The measured IDD values when the IMBP is put into Low-Power Stop mode with the EXTAL pin stopped in either the low or high state and the device having previously entered Low-Power Standby mode are given in Table 4.

Table 4 Low-Power Stop Mode Idd Measurements

EXTAL Freq	Vdd	Low-Power Stop IDD
0 Hz (DC)	5 V	52 uA
0 Hz (DC)	3.3 V	20 uA

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