

COMexpress Development System Carrier Errata

1 Overview

Last Update: 2011 FEB 23

This document describes the known errata and limitations of the COM Express DS Carrier for P2020COMe-DS-PB kit Development System. In all cases, if an errata has a work-around, it is applied to the system before being shipped to customers.

The assembly revision is updated every time a new problem or system upgrade is found and systems have been shipped. The first fabbed board revision is rev. A. After a re-spin, valid assembly rev is updated to be are “ B, C, D”... and so on. If your current assembly revision is rev “B”, then it has all rev “B” fixes along with all the rev A, as well as all the previous pre-production fixes. A rev “B” assembly would not have any of the rev “C” fixes. Look for the sticker 700-xxxx rev. X to see what revision to which the errata is applied.

Regarding the published schematics, the schematic history section found on sheet #2 denotes which errata have been incorporated into the schematic. If no history is present, then no errata has yet been incorporated into the schematic. In such cases, the errata should be applied to the published schematics to determine the correct wiring of the system (i.e. after the changes are applied).+

2 Summary Descriptions

The following table describes the errata, including date discovered and PCB assembly revisions for which the errata may be applicable. For those errata which have a work-around, consult the PCB label for information.

Table 1: COM Express DS Carrier for P2020COMe-DS-PB kit Errata

Errata	Rev. Applied To	Problem / Respin Resolution	Errata Correction/ Work-around
E1 11FEB23	A, B	SPI chip on carrier shares the same CS0 as P2020 module's SPI chip; thus, system is default to carrier SPI chip instead of SPI chip on module.	Use the SPI chip on carrier since it is bigger. Rev. C will change chip select to CS1 for the carrier chip.

3 Changes

Rev	Date	Changes
1	2011FEB23	Initial Errata
2		
3		
4		
5		
6		

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