



**MOTOROLA**

Chip Errata  
**DSP56007 Digital Signal Processor**  
 Mask: 0F91R

**ERRATA**

Errata Description

Applies  
 to Mask

1. Specification timings #83, #84, and #87 in the data sheet provide  $1 \times T_C$  less than specified; e.g.,
  - a. specification #83 measures  $8 \times T_C$  ( $12 \times T_C$ ) instead of  $9 \times T_C$  ( $13 \times T_C$ ) in the EMI fast (slow) DRAM timing mode, respectively;
  - b. specification #84 measures  $4 \times T_C - 9$  ( $6 \times T_C - 9$ ) instead of  $5 \times T_C - 9$  ( $7 \times T_C - 9$ ) in the EMI fast (slow) DRAM timing mode, respectively; and
  - c. specification #87 measures  $4 \times T_C - 15$  ( $6 \times T_C - 15$ ) instead of  $5 \times T_C - 15$  ( $7 \times T_C - 15$ ) in the EMI fast (slow) DRAM timing mode, respectively.

0F91R

**Workaround:** The refresh  $t_{RAS}$  timing requirement in a 60 ns DRAM device is not met when the DSP56007FJ66 runs at full speed (66 MHz) and the EMI is programmed in the "fast" DRAM timing mode (EDTM = 0 in ECSR). In this case, only spec timing #84 does not meet the requirement. To ensure correct refresh of a 60 ns DRAM connected to DSP56007FJ66 running at 66 MHz and accessing the DRAM using the EMI fast timing mode, one of the following methods is recommended:

- a. Access the DRAM device without using the internal refresh timer, as described in Section 3.4.1 of the user's manual. This method is possible if the data transfer rate is high.
- b. Refresh the DRAM device in a burst manner, as described in Section 3.4.2.2 of the user's manual. This method divides the real time audio processing window into two portions.

During the first portion, DRAM data transfers without refresh (EREF = 0) are done using the EMI fast timing mode (EDTM = 0).

During the second portion, when EMI is not doing data transfers, a burst of refresh cycles is enabled (EREF = 1) using the EMI slow timing mode (EDTM = 1).



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<u>Errata Description</u>	<u>Applies to Mask</u>
2. Chips marked as 0F91R will not boot properly through the Serial Host Interface (SHI). Use either the OnCE port or the External Memory Interface (EMI) to bootstrap these chips.	0F91R



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**NOTES**

- 1. An over-bar (for example,  $\overline{\text{xxxx}}$ ) indicates an active-low signal.
- 2. The letters seen to the right of the errata tell which DSP56007 mask numbers apply.

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