MOTOROLA

Chip Errata
DSP56156 Digital Signal Processor
Mask: E69A

ERRATA

Errata Description	Applies to Mask
1. There are three speed grades of the 1E69A silicon of the DSP56156: 40 MHz, 50 MHz and 60 MHz. These three speed grades are tested as shown in the table below.	D13N E69A

Table 1: 1E69A Marking and Testing Conditions

Characteristic	Symbol	40 MHz		50 MHz		60 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Supply Voltage	V_{CC}	4.75	5.25	4.75	5.25	4.75	5.25	V
Junction Temperature	T_J	—	115	—	115	—	115	°C

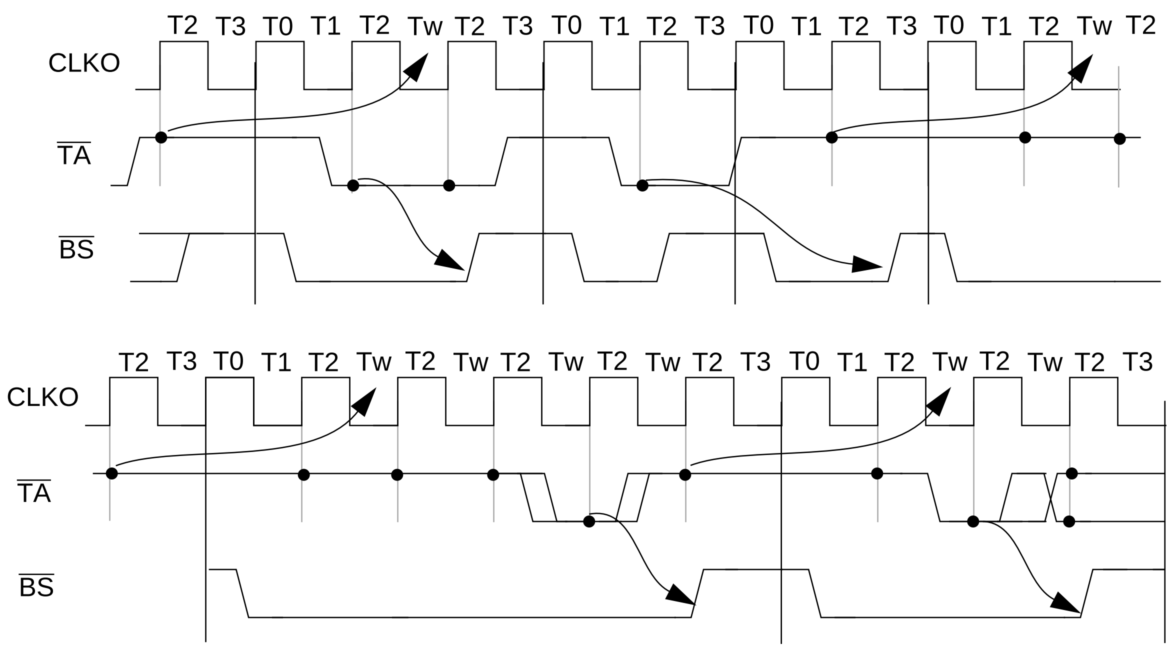
The PLL is functional and tested at 60 MHz for the speed grades.

The codec is functional and tested with a 20 MHz external clock, 0 dB gain on the A/D input and D/A output, 128 decimation ratio. The A/D is tested with a 0.4 Vrms signal at 1.5 KHz and the D/A with a digitally generated sine wave 50% full scale at 2 KHz. Under those conditions, the SNR and THD of the A/D and D/A are better than 60 dB.

Errata Description	Applies to Mask
2. In master mode (MODC=1), a bus conflict during multiple external bus accesses will translate into incorrect external data transfer. Following are two examples under which this problem will occur: External data memory access in mode 3 master mode (MODC=1; MODB=1; MODA=1); Dual external data memory access in mode 2 master mode (MODC=1; MODB=1; MODA=0).	E69A
3. The OnCE pins OS1 and OS0 will not display the status of the chip correctly when in the wait condition (executing wait states because the current bus cycle hasn't completed due to $\overline{BG}$ or $\overline{TA}$).	D13N D89T E69A
4. The $\overline{TA}$ pin behavior of this mask set (as well as all previous mask sets) does not match the $\overline{TA}$ definition described in the DSP56156 data sheet (2/1/92). The $\overline{TA}$ behavior is described below; it will be changed to the behavior described in the data sheet in a later revision of the silicon:	D13N D89T E69A

Errata Description	Applies to Mask

$\overline{\text{TA}}$ (Transfer Acknowledge) - active low input. If there is no external bus activity, the $\overline{\text{TA}}$ input is ignored by the DSP. When there is external bus cycle activity, $\overline{\text{TA}}$ can be used to insert wait states in the external bus cycle. $\overline{\text{TA}}$ is sampled on the leading edge of T2. Any number of wait states from 1 to infinity may be inserted by using $\overline{\text{TA}}$. If $\overline{\text{TA}}$ is sampled high one clock period before the beginning of a bus cycle, at least one wait states will be inserted in the bus cycle. The bus cycle will end 4T after the $\overline{\text{TA}}$ has been sampled low on a leading edge of the clock, if the Bus Control Register (BCR) value does not program more wait states. The number of wait states is determined by the $\overline{\text{TA}}$ input or by the BCR, whichever is longer. $\overline{\text{TA}}$ is still sampled during the leading edge of the clock when wait states are controlled by the BCR value. In that case, $\overline{\text{TA}}$ will have to be sampled low during the leading edge of the last wait state programmed by the BCR (4T before the end of the bus cycle programmed by the BCR) in order not to add any wait states. If $\overline{\text{TA}}$ is sampled low (asserted) at the leading edge of T2 preceding the bus cycle, and if no wait states are specified in the BCR register, zero wait states will be inserted in the external bus cycle.



$\overline{\text{TA}}$ Controlled Accesses

5. At higher voltages, the TFS bit in the SSI's status register will not be set under all conditions when it would normally be set. The actual voltage at where this failure occurs is process dependent, and can fail at voltages as low as 4.7 V and above, depending on the processing. This failure is independent of temperature and frequency. — D13N, D89T, E69A

Errata Description	Applies to Mask
6. The BRKcc instruction will not operate correctly and will not exit a DO loop when it is immediately followed by an instruction which causes contention (note that if the brkcc instruction is at the end of a loop, the instruction which immediately follows can be the instruction at the top of the loop). This happens in the following cases:	E69A

1. Instruction after BRKcc accesses external memory and another processor arbitrates for and gets the bus.
2. Instruction after BRKcc is a dual read, both reads from external memory.
3. Instructions are located off-chip and the instruction after BRKcc accesses external memory.
4. Instructions are located off-chip and another processor arbitrates for and gets the bus.

In the first three cases, the problem can be fixed by guaranteeing that the instruction immediately after the BRKcc does not access external memory. For the case where the instructions are located off-chip and another processor can arbitrate for the bus, the BRKcc instruction may not be used.

The BRKcc functionality may be emulated in software as follows:

```
        do      #5,label
         .
         .
        bpl     exitlp          ; used to emulate BRKcc
         .
label
        bra     over            ; used to emulate BRKcc
exitlp
        enddo                   ; used to emulate BRKcc
over
```

7. The DO instruction, in the special case when using a register or memory location as the loop count and the value is zero, will not operate correctly when it is immediately preceded by an instruction which causes contention. This happens in the following cases:	E69A

1. Instruction before DO accesses external memory and another processor arbitrates for and gets the bus.
2. Instruction before DO is dual read, both reads from external memory.
3. Instructions are located off-chip and the instruction before DO accesses external memory.
4. Instructions are located off-chip and another processor arbitrates for and gets the bus as the DO executes.

Errata Description	Applies to Mask
In the first three cases, the problem can be fixed by guaranteeing that the instruction before the DO does not access external memory. For the case where the instructions are located off-chip and another processor can arbitrate for the bus, the software fix above (see item 6.) must be used. Note that these problems do not apply anytime it can be guaranteed that the loop count is not zero.The functionality of a DO with loop count of zero may be emulated by testing the value of the register or memory location first to determine if the loop count is zero, and if it is zero, then to branch over the loop.	
8. If the master mode is selected after power up reset (MODC pin pulled up) and if the bootstrap mode is selected (MODB pin pulled down), the chip will be set in the slave mode by the last instruction of the bootstrap program (MC bit of the OMR written to 0). The MC bit of the OMR can be written to 1 by the first instruction of the internal program RAM to select back the master mode before any external access.	E69A
9. The $\overline{BS}$ signal is being deasserted before $\overline{TA}$ is deasserted if the BCR is programmed for one or more wait states. In this case, the $\overline{BS}$ signal ignores the $\overline{TA}$ signal and is deasserted under control of the BCR even though $\overline{TA}$ is still active and should cause $\overline{BS}$ to remain active. This problem occurs at: $f_{OSC} = 60$ MHz, $T_J \geq 25$ °C, $V_{CC} \leq 5$ V This problem has not been reported on parts rated at less than 60 MHz, although it has been seen at 50 MHz at 5 V and may be appear at other speeds. The temporary solution is to use either the BCR register or the $\overline{TA}$ signal to insert wait states but not both.	D13N D89T E69A F44E E98S
10. The lock bit detection circuitry in the PLL fails to operate correctly in an overdamped system. A work around is to use a smaller capacitance value for the SXFC capacitor to GND. However reducing this capacitor value will increase PLL jitter. If jitter is found to be unacceptable then it is recommened to switch to a larger capacitance once the lock bit has been asserted. If this (hardware) fix cannot be done then the operating software for the device must be changed from a polling technique on the lock bit to simply waiting for 5mS for the PLL to lock before enabling the PLL to the core.	D13N D89T E69A F44E E98S

NOTES

1. An over-bar (i.e. $\overline{xxxx}$) indicates an active-low signal.
2. The letters seen to the right of the errata tell which DSP56156 mask numbers apply.
3. Manuals and data sheets may also have errata that is documented on the appropriate errata sheet as discovered.

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