

ES_LPC11E6x

Errata sheet LPC11E6x

Rev. 1.1 — 23 October 2015

Errata sheet

Document information

Info	Content
Keywords	LPC11E67JBD48; LPC11E68JBD64; LPC11E68JBD100, LPC11E6x errata
Abstract	<p>This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document.</p> <p>Each deviation is assigned a number and its history is tracked in a table.</p>



Revision history

Rev	Date	Description
1.1	20151023	<ul style="list-style-type: none">Added UART.1
1	20140401	<ul style="list-style-type: none">Initial version.

Contact information

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1. Product identification

The LPC11E6x devices typically have the following top-side marking for LQFP100 packages:

LPC11E6xJBD100
 xxxxxx xx
 xxxyywwxR[x]

The LPC11E6x devices typically have the following top-side marking for LQFP64 packages:

LPC11E6xJ
 xxxxxx xx
 xxxyywwxR[x]

The LPC11E6x devices typically have the following top-side marking for LQFP48 packages:

LPC11E6xJ
 xx xx
 xxxyy
 wwR[x]

Field 'yy' states the year the device was manufactured. Field 'ww' states the week the device was manufactured during that year.

Field 'R' identifies the device revision. This Errata Sheet covers the following revisions of the LPC11E6x:

Table 1. Device revision table

Revision identifier (R)	Revision description
'A'	Initial device revision

2. Errata overview

Table 2. Errata summary table

Functional problems	Short description	Revision identifier	Detailed description
UART.1	The UART controller sets the Idle status bits for receive and transmit before the transmission of the stop bit is complete.	'A'	Section 3.1

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

Table 4. Errata notes table

Errata notes	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

3. Functional problems detail

3.1 UART.1

Introduction:

In receive mode, the UART controller provides a status bit (the RXIDLE bit in the UART STAT register) to check whether the receiver is currently receiving data. If RXIDLE is set, the receiver indicates it is idle and does not receive data.

In transmit mode, the UART controller provides two status bits (TXIDLE and TXDISSTAT bits in the UART STAT register) to indicate whether the transmitter is currently transmitting data. The TXIDLE bit is set by the controller after the last stop bit has been transmitted. The TXDISSTAT bit is set by the controller after the transmitter has sent the last stop bit and has become fully idle following a transmit disable executed by setting the TXDIS bit in the UART CTRL register.

The status bits can be used to implement software flow control, but their setting does not affect normal UART operation.

Problem:

The RXIDLE bit is incorrectly set for a fraction of the clock cycle between the reception of the last data bit and the reception of the start bit of the next word, that is while the stop bit is received. RXIDLE is cleared at the beginning of the start bit.

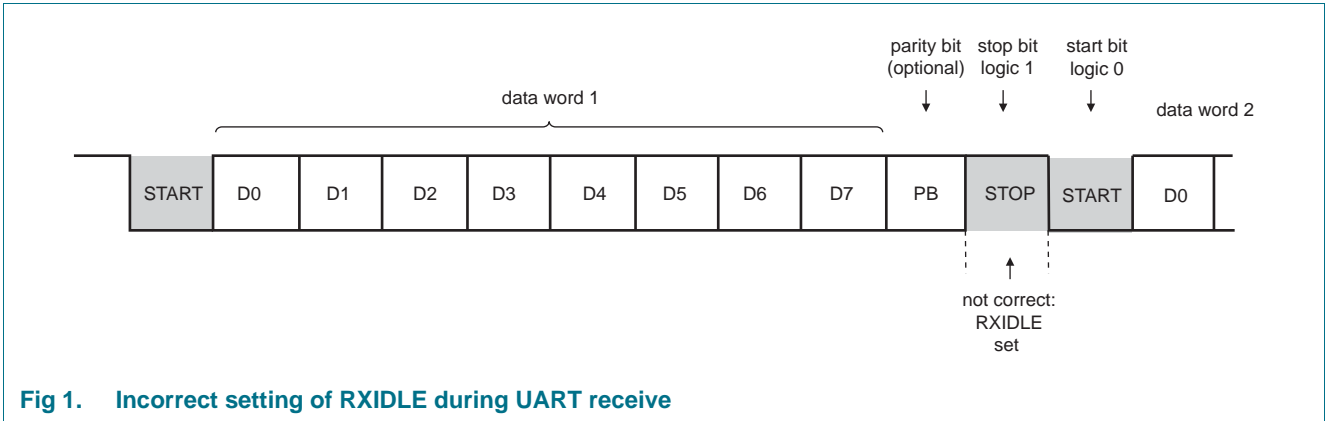


Fig 1. Incorrect setting of RXIDLE during UART receive

Both, TXIDLE and TXDISSTAT are set incorrectly between the last data bit and the stop bit while the transfer is still ongoing.

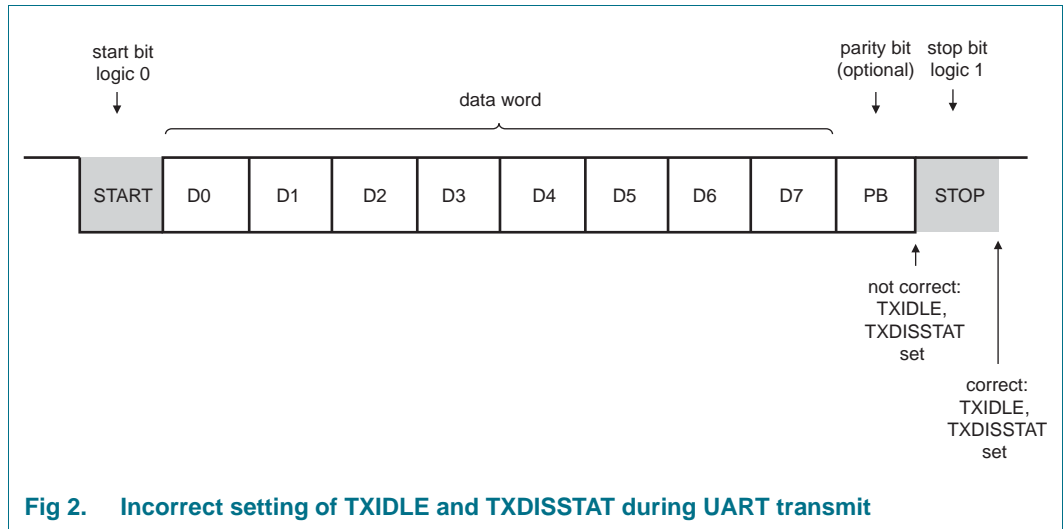


Fig 2. Incorrect setting of TXIDLE and TXDISSTAT during UART transmit

Work-around:

When writing code that checks for the setting of any of the status bits RXIDLE, TXIDLE, TXDISSTAT, check the value of the status bit in the STAT register:

- If status bit = 1, add a delay of one UART bit time (if STOPLEN = 0, one stop bit) or two bit times (if STOPLEN = 1, two stop bits) and check the value of the status bit again:
 - If status bit = 1, the receiver is idle.
 - If status bit = 0, the receiver is receiving data.
- If the status bit = 0, the receiver is receiving data.

4. AC/DC deviations detail

4.1 n/a

5. Errata notes detail

5.1 n/a

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