ES_LPC2194/01

Errata sheet LPC2194/01

Rev. 3 — 1 October 2011 **Errata sheet**

Document information

Info	Content
Keywords	LPC2194/01 errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table.

Revision history

Rev	Date	Description
3	20111001	• Added Rev. D.
2	20110401	• The format of this errata sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Added ADC.1. and Note.2.
1	20070727	• First version.

Contact information

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1. Product identification

The LPC2194/01 devices typically have the following top-side marking:

LPC2194xxxxxx

/01

xxxxxxx

xxYYWW R

The last letter in the last line (field ‘R’) will identify the device revision. This Errata Sheet covers the following revisions of the LPC2194/01:

Table 1. Device revision table

Revision identifier (R)	Revision description
‘C’	First device revision
‘D’	Second device revision

Field ‘YY’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
CORE.1	Incorrect update of the Abort Link register in Thumb state	‘C’, ‘D’	Section 3.1
CAN.1	Data overrun condition can lock the CAN controller	‘C’, ‘D’	Section 3.2
ADC.1	External sync inputs not operational	‘C’, ‘D’	Section 3.3

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Product version(s)	Detailed description
n/a	n/a	n/a	n/a

Table 4. Errata notes table

Errata notes	Short description	Revision identifier	Detailed description
Note.1	New CAN controller with some changes	‘C’, ‘D’	Section 5.1
Note.2	Pin TD1 (pin 10) must not be driven LOW during reset.	‘C’, ‘D’	Section 5.2

3. Functional problems detail

3.1 CORE.1: Incorrect update of the Abort Link register in Thumb state

Introduction:

If the processor is in Thumb state and executing the code sequence STR, STMIA or PUSH followed by a PC relative load, and the STR, STMIA or PUSH is aborted, the PC is saved to the abort link register.

Problem:

In this situation the PC is saved to the abort link register in word resolution, instead of half-word resolution.

Conditions:

The processor must be in Thumb state, and the following sequence must occur:

```
<any instruction>
<STR, STMIA, PUSH> <---- data abort on this instruction
LDR rn, [pc,#offset]
```

In this case the PC is saved to the link register R14_abt in only word resolution, not half-word resolution. The effect is that the link register holds an address that could be #2 less than it should be, so any abort handler could return to one instruction earlier than intended.

Work-around:

In a system that does not use Thumb state, there will be no problem.

In a system that uses Thumb state but does not use data aborts, or does not try to use data aborts in a recoverable manner, there will be no problem.

Otherwise the workaround is to ensure that a STR, STMIA or PUSH cannot precede a PC-relative load. One method for this is to add a NOP before any PC-relative load instruction. However this would have to be done manually.

3.2 CAN.1: Data Overrun condition can lock the CAN controller

Introduction:

Each CAN controller provides a double Receive Buffer (RBX) per CAN channel to store incoming messages until they are processed by the CPU. Software task should read and save received data as soon as a message reception is signaled.

In cases where both receive buffers are filled and the contents are not read before the third message comes in, a CAN Data Overrun situation is signaled. This condition is signaled via the Status register and the Data Overrun Interrupt (if enabled).

Problem:

In a Data Overrun condition, the CAN controller is locked from further message reception.

Work-around:

1. Recovering from this situation is only possible with a soft reset to the CAN controller.
2. If software cannot read all messages in time before a third message comes in, it is recommend to change the acceptance filtering by adding further acceptance filter group(s) for messages, which are normally rejected. With this approach, the third incoming message is accepted and the Data Overrun condition is avoided. These additional messages are received with the corresponding group index number can be easily identified and rejected by software.

3.3 ADC.1: External sync inputs not operational

Introduction:

In software-controlled mode (BURST bit is 0), the 10-bit ADC can start conversion by using the following options in the A/D Control Register:

26:24	START		When the BURST bit is 0, these bits control whether and when an ADC conversion is started:	0
		000	No start (this value should be used when clearing PDN to 0).	
		001	Start conversion now.	
		010	Start conversion when the edge selected by bit 27 occurs on P0.16/EINT0/MAT0.2/CAP0.2 pin.	
		011	Start conversion when the edge selected by bit 27 occurs on P0.22/CAP0.0/MAT0.0 pin.	
		100	Start conversion when the edge selected by bit 27 occurs on MAT0.1.	
		101	Start conversion when the edge selected by bit 27 occurs on MAT0.3.	
		110	Start conversion when the edge selected by bit 27 occurs on MAT1.0.	
		111	Start conversion when the edge selected by bit 27 occurs on MAT1.1.	

Fig 1. A/D control register options

Problem:

The external start conversion feature, ADCR:START = 0x2 or 0x3, may not work reliably and ADC external trigger edges on P0.16 or P0.22 may be missed. The occurrence of this problem is peripheral clock (pclk) dependent. The probability of error (missing a ADC trigger from GPIO) is estimated as follows:

- For PCLK_ADC = 60 MHz, probability error = 12 %
- For PCLK_ADC = 50 MHz, probability error = 6 %
- For PCLK_ADC = 12 MHz, probability error = 1.5 %

The probability of error is not affected by the frequency of ADC start conversion edges.

Work-around:

In software-controlled mode (BURST bit is 0), the START conversion options (bits 26:24 set to 0x1 or 0x4 or 0x5 or 0x6 or 0x7) can be used. The user can also start a conversion by connecting an external trigger signal to a capture input pin (CAPx) from a Timer peripheral to generate an interrupt. The timer interrupt routine can then start the ADC conversion by setting the START bits (26:24) to 0x1. The trigger can also be generated from a timer match register.

4. AC/DC deviations detail

4.1 n/a

5. Errata notes detail

5.1 Note.1

The CAN controller on the LPC2194/01 is a new certified CAN controller. This controller has an improved interrupt behavior in Full-CAN mode. Care should be taken while using the global CAN filter look-up table (LUT). In the old CAN block (as found in the LPC2194, and LPC2194/00), the numbering of the CAN interfaces in the LUT is 1 to n. In the new CAN block, the numbering of the CAN interfaces in the LUT is 0 to n-1 (n being the number of implemented CAN interfaces (2 or 4)).

5.2 Note.2

Pin TD1 (pin 10) must not be driven LOW during reset. If LOW on reset the device behavior is undetermined.

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