

ES_LPC2220

Errata sheet LPC2220

Rev. 2 — 1 April 2011

Errata sheet

Document information

Info	Content
Keywords	LPC2220 errata
Abstract	<p>This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document.</p> <p>Each deviation is assigned a number and its history is tracked in a table.</p>



Revision history

Rev	Date	Description
2	20110401	<ul style="list-style-type: none">The format of this errata sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.Added ADC.1.
1.5	20080305	<ul style="list-style-type: none">Previous version.

Contact information

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1. Product identification

The LPC2220 devices typically have the following top-side marking:

```
LPC2220xxx
xxxxxxx
xxYYWW R
```

The last letter in the last line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the LPC2220:

Table 1. Device revision table

Revision identifier (R)	Revision description
'.'	Initial device revision
'B'	Second device revision
'C'	Third device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
CORE.1	Incorrect load of the link register	',' , 'B' , 'C'	Section 3.1
SPI.1	Incorrect shifting of data in slave mode at lower frequencies	',' , 'B'	Section 3.2
SSP.1	Initial data bits/clocks corrupted in SSP transmission	',' , 'B' , 'C'	Section 3.3
Timer0.1	Match 0.1 is not connected to P0.5	',' , 'B'	Section 3.4
Timer.1	Timer Counter reset occurs on incorrect edge in counter mode	',' , 'B' , 'C'	Section 3.5
ADC.1	External sync inputs not operational	',' , 'B' , 'C'	Section 3.6

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Product version(s)	Detailed description
n/a	n/a	n/a	n/a

Table 4. Errata notes table

Errata notes	Short description	Revision identifier	Detailed description
Note.1	Pin n.c. (pin 22, H2) must not be driven low during reset	',' , 'B' , 'C'	Section 5.1

3. Functional problems detail

3.1 Core.1: Incorrect update of the Abort Link register in Thumb state

Introduction:

If the processor is in Thumb state and executing the code sequence STR, STMIA or PUSH followed by a PC relative load, and the STR, STMIA or PUSH is aborted, the PC is saved to the abort link register.

Problem:

In this situation the PC is saved to the abort link register in word resolution, instead of half-word resolution.

Conditions:

The processor must be in Thumb state, and the following sequence must occur:

```
<any instruction>  
<STR, STMIA, PUSH> <---- data abort on this instruction  
LDR rn, [pc,#offset]
```

In this case the PC is saved to the link register R14_abt in only word resolution, not half-word resolution. The effect is that the link register holds an address that could be #2 less than it should be, so any abort handler could return to one instruction earlier than intended.

Work-around:

In a system that does not use Thumb state, there will be no problem.

In a system that uses Thumb state but does not use data aborts, or does not try to use data aborts in a recoverable manner, there will be no problem.

Otherwise the workaround is to ensure that a STR, STMIA or PUSH cannot precede a PC-relative load. One method for this is to add a NOP before any PC-relative load instruction. However this would have to be done manually.

3.2 SPI.1: Incorrect shifting of data in slave mode at lower frequencies

Introduction:

In slave mode, the SPI can set the clock phase (CPHA) to 0 or 1.

Problem:

Consider the following conditions:

1. SPI is configured as a slave (with CPHA=0).
2. SPI is running at a low frequency.

In slave mode, the SPIF (SPI Transfer Complete Flag) bit is set on the last sampling edge of SCK. If CPHA is set to 0 then the last sampling edge of SCK would be the rising edge.

Under the above conditions, if the SPI Data Register (SPDR) is written to less than a half SCLK cycle after the SPIF bit is set (this would happen if the SPI frequency is low) then the SPDR will shift data one clock early for the upcoming transfers.

Lowering the SPI frequency would increase the likelihood of the SPDR write happening in the first half SCK cycle of the last sampling clock.

Work-around:

There are two possible workarounds:

1. Use CPHA=1.
2. If the data is shifted incorrectly when CPHA is set to 0 then delaying the write to SPDR after the half SCK cycle of the last sampling clock would resolve this issue.

3.3 SSP.1: Initial data bits/clocks of the SSP transmission are shorter than subsequent pulses at higher frequencies

Introduction:

The SSP is a Synchronous Serial Port (SSP) controller capable of operation on a SPI, 4-wire SSI or a Microwire bus. The SSP can operate at a maximum speed of 30 MHz and it referred to as SPI1 in the device documentation.

Problem:

At high SSP frequencies, it is found that the first four pulses are shorter than the subsequent pulses.

At 30 MHz, the first pulse can be expected to be approximately 10 ns shorter and the second pulse around 5 ns shorter. The remaining two pulses are around 2 ns shorter than subsequent pulses.

At 25 MHz, the length of the first pulse would be around 7 ns shorter. The subsequent three pulses are around 2 ns shorter.

At 20 MHz only the first pulse is affected and it is around 2 ns shorter. All subsequent pulses are fine.

The deviation of the initial data bits/clocks will decrease as the SSP frequency decreases.

Work-around:

None.

3.4 Timer0.1: Match 0.1 output cannot be seen on port pin P0.5 if configured as an alternate function

Introduction:

Timer0 has four external match outputs corresponding to match registers with various capabilities. Match 0.0 can be configured as an alternate function on P0.3 and P0.22. Match 0.1 can be configured as an alternate function on Port 0.5 and P0.27. The alternate functions can be configured by using the respective PINSELx register.

Problem:

Match 0.0 should have been only connected to P0.3 and P0.22 but it is also connected to P0.5. Match 0.1 is only connected to P0.27. Hence if the application configures the External Match alternate function on both P0.3 (Match 0.0) and P0.5 (Match 0.1) then the Match 0.0 output can be seen on two port pins, namely P0.3 and P0.5.

Work-around:

Only P0.27 can be used for Match 0.1.

3.5 Timer.1: In counter mode, the Timer Counter reset does not occur on the correct incoming edge

Problem:

Timer0 and Timer1 can be used in a counter mode. In this mode, the Timer Counter register can be incremented on rising, falling or both edges which occur on a selected CAP input pin.

This counter mode can be combined with the match functionality to provide additional features. One of the features would be to reset the Timer Counter register on a match. The same would also apply for Timer1.

Work-around:

There are two possible workarounds:

1. Combine the Timer Counter reset feature with the “interrupt on match” feature. The interrupt on match occurs on the correct incoming edge. In the ISR, the Timer Counter register can also be reset. This solution can only work if no edges are expected during the duration of the ISR.
2. In this solution, the “interrupt on match” feature is not used. Instead, the following specific initialization can achieve the counting operation:
 - a. Initialize the Timer Counter register to 0xFFFFFFFF.
 - b. If “n” edges have to be counted then initialize the corresponding Match register with value n-1. For instance, if 2 edges need to be counted then load the Match register with value 1.

More details on the above example:

1. Edge 1 - Timer overflows and Timer Counter (TC) is set to 0.
2. Edge 2 - TC=1. Match takes place.
3. Edge 3 - TC=0.
4. Edge 4 - TC=1. Match takes place.
5. Edge 5 - TC=0.

3.6 ADC.1: External sync inputs not operational

Introduction:

In software-controlled mode (BURST bit is 0), the 10-bit ADC can start conversion by using the following options in the A/D Control Register:

26:24	START	When the BURST bit is 0, these bits control whether and when an ADC conversion is started:	0
	000	No start (this value should be used when clearing PDN to 0).	
	001	Start conversion now.	
	010	Start conversion when the edge selected by bit 27 occurs on P0.16/EINT0/MAT0.2/CAP0.2 pin.	
	011	Start conversion when the edge selected by bit 27 occurs on P0.22/CAP0.0/MAT0.0 pin.	
	100	Start conversion when the edge selected by bit 27 occurs on MAT0.1.	
	101	Start conversion when the edge selected by bit 27 occurs on MAT0.3.	
	110	Start conversion when the edge selected by bit 27 occurs on MAT1.0.	
	111	Start conversion when the edge selected by bit 27 occurs on MAT1.1.	

Fig 1. A/D control register options

Problem:

The external start conversion feature, ADCR:START = 0x2 or 0x3, may not work reliably and ADC external trigger edges on P0.16 or P0.22 may be missed. The occurrence of this problem is peripheral clock (pclk) dependent. The probability of error (missing a ADC trigger from GPIO) is estimated as follows:

- For PCLK_ADC = 60 MHz, probability error = 12 %
- For PCLK_ADC = 50 MHz, probability error = 6 %
- For PCLK_ADC = 12 MHz, probability error = 1.5 %

The probability of error is not affected by the frequency of ADC start conversion edges.

Work-around:

In software-controlled mode (BURST bit is 0), the START conversion options (bits 26:24 set to 0x1 or 0x4 or 0x5 or 0x6 or 0x7) can be used. The user can also start a conversion by connecting an external trigger signal to a capture input pin (CAPx) from a Timer peripheral to generate an interrupt. The timer interrupt routine can then start the ADC conversion by setting the START bits (26:24) to 0x1. The trigger can also be generated from a timer match register.

4. AC/DC deviations detail

4.1 n/a

5. Errata notes detail

5.1 Note.1

Pin n.c. (pin 22, H2) must not be driven low during reset. If low on reset the device behavior is undetermined.

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