## Document information

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<th>Info</th>
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<tr>
<td>Keywords</td>
<td>LPC54102J512UK49; LPC54102J256UK49; LPC54101J512UK49; LPC54101J256UK49;</td>
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<td>LPC54101J256BD64; LPC54102J512BD64; LPC54102J256BD64; LPC54101J512BD64;</td>
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<td>LPC54101J256BD64; LPC54101J256BD64</td>
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<tr>
<td>Abstract</td>
<td>LPC5410x errata</td>
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## Revision history

<table>
<thead>
<tr>
<th>Rev</th>
<th>Date</th>
<th>Description</th>
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<tbody>
<tr>
<td>2.3</td>
<td>20171121</td>
<td>• Added IRC.1</td>
</tr>
<tr>
<td>2.2</td>
<td>20170421</td>
<td>• Added CRP.1</td>
</tr>
<tr>
<td>2.1</td>
<td>20151216</td>
<td>• Power ROM API.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Updated Section 1 “Product identification”. Added boot code revision.</td>
</tr>
<tr>
<td>2.0</td>
<td>20150501</td>
<td>• Added RTC.1</td>
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<td></td>
<td></td>
<td>• Added ISP.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Frequency.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Updated product identification information</td>
</tr>
<tr>
<td>1</td>
<td>20141105</td>
<td>• Initial version</td>
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</table>

## Contact information

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For sales office addresses, please send an email to: salesaddresses@nxp.com
1. Product identification

The ES_LPC5410x LQFP64 package has the following top-side marking:

- First line: LPC5410xJyyy
  - x: 2 = dual core (M4, M0+), 1 = single core (M4)
  - yyy: flash size
- Second line: BD64
- Third line: xxxxxxxxxxx
- Fourth line: xxyywwx[R]z
  - yyyw: Date code with yy = year and ww = week.
  - xR = boot code version and device revision.

The ES_LPC5410x WLCSP49 package has the following top-side marking:

- First line: LPC5410x
  - x: 2 = dual core (M4, M0+), 1 = single core (M4)
- Second line: JxxxUK49
  - xxx: flash size
- Third line: xxxxxxxx
- Fourth line: xxyyww
  - yyyw: Date code with yy = year and ww = week.
- Fifth line: xxxxx
- Sixth line: NXP x[R]z
  - xR = boot code version and device revision.

This Errata Sheet covers the following revisions of the LPC5410x:

<table>
<thead>
<tr>
<th>Revision identifier (R)</th>
<th>Revision description</th>
</tr>
</thead>
<tbody>
<tr>
<td>'1B'</td>
<td>Initial device revision with boot code version 17.1.</td>
</tr>
<tr>
<td>'1C'</td>
<td>Second device revision with boot code version 17.1.</td>
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# 2. Errata overview

## Table 2. Functional problems table

<table>
<thead>
<tr>
<th>Functional problems</th>
<th>Short description</th>
<th>Revision identifier</th>
<th>Detailed description</th>
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</thead>
<tbody>
<tr>
<td>RTC.1</td>
<td>The PDEN_32K_OSC bit gets cleared when the MCU wakes up from Deep power-down mode. This causes the RTC oscillator to change from bypass mode to crystal mode.</td>
<td>‘1B’, ‘1C’</td>
<td>Section 3.1</td>
</tr>
<tr>
<td>ISP.1</td>
<td>ISP (In-System Programming) command for UID (unique identification number) is not functional.</td>
<td>‘1B’, ‘1C’</td>
<td>Section 3.2</td>
</tr>
<tr>
<td>Frequency.1</td>
<td>The maximum operating system clock on the LPC5410x device is limited to 96 MHz.</td>
<td>‘1B’</td>
<td>Section 3.3</td>
</tr>
<tr>
<td>POWER_API.1</td>
<td>The set-voltage ROM API call does not configure the internal regulator correctly for the desired operating frequency.</td>
<td>‘1B’, ‘1C’</td>
<td>Section 3.4</td>
</tr>
<tr>
<td>CRP.1</td>
<td>Code read protection level 1 is not functional.</td>
<td>‘1B’, ‘1C’</td>
<td>Section 3.5</td>
</tr>
<tr>
<td>IRC.1</td>
<td>Accuracy of the Internal RC Oscillator (IRC) frequency for the LPC5410x Revision B devices in the WLCSP49 package are outside of the IRC specification</td>
<td>‘1B’</td>
<td>Section 3.6</td>
</tr>
</tbody>
</table>

## Table 3. AC/DC deviations table

<table>
<thead>
<tr>
<th>AC/DC deviations</th>
<th>Short description</th>
<th>Revision identifier</th>
<th>Detailed description</th>
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</thead>
<tbody>
<tr>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
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</tbody>
</table>

## Table 4. Errata notes

<table>
<thead>
<tr>
<th>Note</th>
<th>Short description</th>
<th>Revision identifier</th>
<th>Detailed description</th>
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<tbody>
<tr>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
</tr>
</tbody>
</table>
3. Functional problems detail

3.1 RTC.1: The RTC oscillator changes from bypass control mode to crystal mode when waking up from Deep power-down mode.

Introduction:

On the LPC5410x, the low power 32 KHz RTC oscillator can be configured to run in crystal oscillation mode or bypass control mode. In crystal oscillation mode, the RTC oscillator is driven by an external 32 KHz crystal and in bypass control mode, the RTC oscillator is driven by an external 32 KHz clock. Bypass control mode can be entered by setting the PDEN_32K_OSC bit in the PDRUNCFG register (bit 24).

Problem:

The PDEN_32K_OSC bit gets cleared when the MCU wakes up from Deep power-down mode. This causes the RTC oscillator to change from bypass mode to crystal mode.

Work-around:

If using deep power-down mode, the crystal oscillation mode should be used instead of the bypass crystal mode. The bypass crystal mode can be used in active, sleep, deep-sleep, and power-down modes.

3.2 ISP.1: ISP (In-System Programming) command for UID (unique identification number) is not functional.

Introduction:

Each LPC5410x device contains a device serial number (four 32-bit words) for unique identification. The ISP call (ReadUID) can be performed via the USART interface to read the unique serial number where the word at the lowest address is sent first.

Problem:

On the LPC5410x, the read UID ISP command is not functional.

Work-around:

The unique serial number (four 32-bit words) can be directly read from address locations 0x01800100 to 0x0180010C.
3.3 Frequency: The maximum operating system clock on the LPC5410x device is limited to 96 MHz.

Introduction:
The LPC5410x data sheet specifies that the LPC5410x device can operate at CPU frequencies up to 100 MHz.

Problem:
To guard band for process, voltage, and temperature, the operating frequency is limited to \( \leq 96 \) MHz.

Work-around:
None. Use CPU frequencies \( \leq 96 \) MHz.

3.4 POWER_API: The set-voltage API ROM call does not configure the internal regulator correctly for the desired operating frequency.

Introduction:
On the LPC5410x device, the following power API ROM calls are provided to configure the system clock, and to manage the power consumption:

- set_pll: Configures the system PLL.
- set_voltage: Controls the device power consumption and the internal regulator for desired operating frequency.
- power_mode_configure: Entry to and wake up from the low power modes.

Problem:
The set-voltage API ROM call does not configure the internal regulator correctly for the desired operating frequency.

Work-around:
The power API library (power_lib) provided in NXP’s LPC5410x LPCOpen v3.xx software platform must be used when calling the set_voltage API call. This library correctly configures the internal regulator for the desired operating frequency.
3.5 CRP.1: Code read protection level 1 is not functional

Introduction:

Code Read Protection is a mechanism that allows the user to enable different levels of security in the system so that access to the on-chip flash and use of the ISP can be restricted. When needed, CRP is invoked by programming a specific pattern in the flash image at offset 0x0000 02FC. There are three levels of code read protection available to the user.

For CRP1 level, erase page command can erase pages in sector 0 only when all pages in the user flash are selected for erase.

Problem:

All pages in sector 0 except page 0 can be erased, which results in erasing CRP1 level.

Work-around:

Use CRP2 level or CRP3 level for code read protection.
3.6 IRC.1: Accuracy of the Internal RC Oscillator (IRC) frequency for the LPC5410x revision B devices in the WLCSP49 package are outside of the IRC specification

Introduction:

The LPC5410x device has a 12 MHz internal RC oscillator (IRC) which can be optionally used as the CPU clock source or as the clock that drives the PLL and subsequently the CPU. The IRC frequency specification in Table 5 is in the LPC5410x data sheet:

Table 5. Dynamic characteristic: IRC oscillator

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ[1]</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{\text{osc(RC)}} )</td>
<td>internal RC oscillator frequency</td>
<td>( T_{\text{amb}} = 25 ^\circ \text{C} )</td>
<td>[2]</td>
<td>12 - 1%</td>
<td>12</td>
<td>12 +1%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( -40 ^\circ \text{C} \leq T_{\text{amb}} \leq +105 ^\circ \text{C} )</td>
<td>[3]</td>
<td>12 -3.5%</td>
<td>12</td>
<td>12 +3%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 0 ^\circ \text{C} \leq T_{\text{amb}} \leq +85 ^\circ \text{C} )</td>
<td>[3]</td>
<td>12 -2%</td>
<td>12</td>
<td>12 +2.5%</td>
</tr>
</tbody>
</table>

[1] Typical ratings are not guaranteed. The value listed is at room temperature (25 °C).

Problem:

For the LPC5410x revision B devices in the WLCSP49 package, the IRC does not meet the limits specified in the LPC5410x data sheet. For temperature range -40 C to 0 C and +85 C to +105 C, this may affect the auto-baud routine's ability to synchronize with the host via serial port 0 during In-System Programming (ISP) at higher baud rates. Table 6 shows the IRC specification for the LPC5410x revision B devices in the WLCSP49 package. This does not affect the LPC5410x devices in the LQFP64 package.

Table 6. Dynamic characteristic: IRC oscillator for revision B devices in WLCSP49 package

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ[1]</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{\text{osc(RC)}} )</td>
<td>internal RC oscillator frequency</td>
<td>( T_{\text{amb}} = 25 ^\circ \text{C} )</td>
<td>12</td>
<td>-2%</td>
<td>12</td>
<td>12 +2%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( -40 ^\circ \text{C} \leq T_{\text{amb}} \leq +105 ^\circ \text{C} )</td>
<td>12</td>
<td>-7%</td>
<td>-</td>
<td>12 +6%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( -20 ^\circ \text{C} \leq T_{\text{amb}} \leq +85 ^\circ \text{C} )</td>
<td>12</td>
<td>-5.5%</td>
<td>-</td>
<td>12 +5%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 0 ^\circ \text{C} \leq T_{\text{amb}} \leq +85 ^\circ \text{C} )</td>
<td>12</td>
<td>-4%</td>
<td>-</td>
<td>12 +3.5%</td>
</tr>
</tbody>
</table>

[1] Typical ratings are not guaranteed. The value listed is at room temperature (25 °C).

Work-around:

This issue will be fixed in the next device revision C.
4. AC/DC deviations detail

No known errata.

5. Errata notes

No known errata.
6. Legal information

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