ERRATA SHEET

Date: **2005 Apr 04**
Document Release: **Version 1.0**
Device Affected: **P89LPC936**

This errata sheet describes both the functional deviations and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

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Identification:

The typical P89LPC936 devices have the following top-side marking:

P89LPC936x x
xxxxxxx xx
xxYYWW R

The last letter in the third line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the P89LPC936:

Revision Identifier (R)	Comment
'A'	Initial device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

Errata Overview - Functional Problems

Functional Problem	Short Description	fixed in revision	added
EEPROM.1	EEPROM lock-up on power up	none	v1.0
DIVM.1	Using DIVM in power-down mode	none	v1.0

Errata Overview - AC/DC Deviations

AC/DC Deviation	Short Description	fixed in revision	added
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Errata Notes

Note	Short Description	added
V_{DD}.1	V_{DD} Power cycling.	v1.0
IRC.1	Internal RC oscillator accuracy.	v1.0

Functional Deviations of P89LPC936

EEPROM.1: EEPROM lock-up on power up

Introduction: The LPC936 has on board data EEPROM, which allows to store non volatile data bytes on the LPC936 that will hold their value when the power is not applied to the LPC936.

Problem: With a slow rising VDD slower than 10ms there is a chance that the EERPOM circuitry will lock up, and incorrect data will be read out.

The EEPROM itself still has the correct data.

Workaround: The data EEPROM can be unlocked by a dummy write cycle. The following function shows a dummy write cycle.

```
void dummywrite(void)
{
 DEECON &= 0x0E;                 // EEPROM write mode
 DEEDAT = 0x5A;                  // dummy data
 DEEADR = 0x00;                  // dummy write address 0x000
 while(!(DEECON&0x80))           // wait till interrupt flag is set
 {
 }
}
```

DIVM.1: Using DIVM in power-down mode

Introduction: The LPC936 has a DIVM register that can be used to divide the cclk down. Using DIVM can greatly reduce power when in active mode.

Problem: When DIVM is used in active mode and power-down mode is then entered the LPC936 can not be waken up from power down mode.

Workaround: Before entering powerdown mode set DIVM back to 0x00. This way the LPC936 will be operating full speed for one instruction before entering power-down mode. After the LPC936 has been waken up DIVM can be set back to its original value.

Electrical and Timing Specification Deviations of P89LPC936

No known errata

Errata Notes

V_{DD}.1: V_{DD} Power cycling

To generate a proper Power-On-Reset (POR), V_{DD} must have dropped below 0.2V before being powered back up. Power-cycling without V_{DD} having dropped below 0.2V may result in incorrect Program Counter values.

Please also see the V_{POR} specification in LPC936 Datasheet, DC electrical characteristics. Section 8.15 (Reset) states that during a power cycle, V_{DD} must fall below V_{POR}.

IRC.1: Internal RC oscillator accuracy

To be able to guarantee the Internal RC oscillator accuracy over the full operating range the V_{DD} supply has to be decoupled sufficiently. Sufficient decoupling is dependant on the noise level in the application, typically a 1uF should be suficient for most applications.

Noise on the V_{DD} supply pins can cause the Internal RC oscillator to go slightly outside of the specified range.