

# ES\_P89LPC902

Errata sheet P89LPC902

Rev. 02 — 4 May 2010

Errata sheet

## Document information

Info	Content
<b>Keywords</b>	P89LPC902 errata
<b>Abstract</b>	<p>This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document.</p> <p>Each deviation is assigned a number and its history is tracked in a table at the end of the document.</p>



**Revision history**

Rev	Date	Description
02	20100504	<ul style="list-style-type: none"><li>The format of this errata sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li></ul>

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## 1. Product identification

The P89LPC902 devices typically have the following top-side marking:

```
P89LPC902x x
xxxxxxx xx
xxYYWW R
```

The last letter in the last line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the P89LPC902:

**Table 1. Device revision table**

Revision identifier (R)	Revision description
'.'	Initial device revision
'A'	Second device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

## 2. Errata overview

**Table 2. Functional problems table**

Functional problems	Short description	Fixed in revision
I/O.1	Port 0.0 can draw additional power	'A'
ICP.1	ICP Global Erase	'A'
RESET.1	External reset does not function correctly when using DIVM	'A'
DIVM.1	Using DIVM in power-down mode	none

**Table 3. AC/DC deviations table**

AC/DC deviations	Short description	Fixed in revision
-	-	-

**Table 4. Errata notes**

Note	Short description	Fixed in revision
V <sub>DD</sub> .1	V <sub>DD</sub> power cycling	none
IRC.1	Internal RC oscillator accuracy	none

### 3. Functional problems detail

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#### 3.1 I/O.1: Port 0.0 can draw additional power

**Introduction:**

Port 0.0 is a general purpose I/O pin.

**Problem:**

P0.0 always has an active internal pull-up, which will draw additional power when the port is written low.

**Work-around:**

No known workaround.

#### 3.2 ICP.1: ICP Global Erase

**Introduction:**

The P89LPC902 can be programmed using ICP (In-Circuit Programming). One of the ICP functions is the Erase Global command, which will erase the entire chip including the security bytes and configuration information.

**Problem:**

When giving the Erase Global command through the ICP interface the P89LPC902 will not clear the busy flag and stay busy forever.

**Work-around:**

The workaround can be done in four steps:

Step 1: Shift out the WR\_FMCON command followed by the Erase Global opcode.

Step 2: Wait 5 ms.

Step 3: Do 8 dummy reads with the RD\_FMDATA\_I command.

Step 4: Read FMCON until the busy flag gets cleared.

Please also see [Figure 1](#).

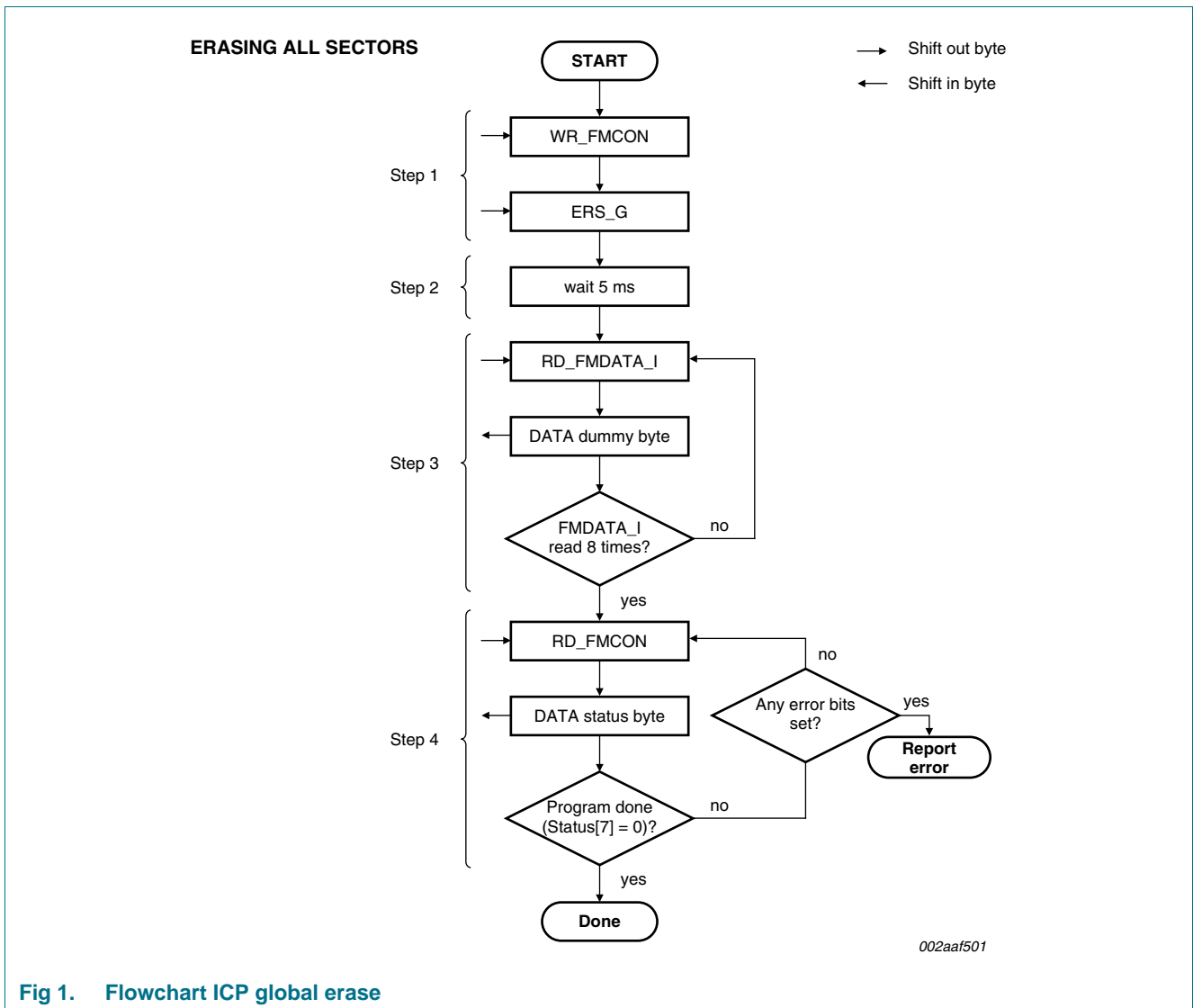


Fig 1. Flowchart ICP global erase

### 3.3 RESET.1: External reset does not function correctly when using DIVM

**Introduction:**

The P89LPC902 can be set up to use either an internal reset or an external reset pin on P1.5. The DIVM register can be used to divide down the internal CCLK down.

**Problem:**

When the P89LPC902 is configured to have an external reset pin on P1.5 and in the program the DIVM register is programmed to a value different from 0x00 to slow down CCLK, then the next reset pulse will not generate a proper reset for the P89LPC902. A power cycle has to be applied for the P89LPC902 to start up again properly.

**Work-around:**

Use the internal reset function.

### 3.4 DIVM.1: Using DIVM in power-down mode

**Introduction:**

The P89LPC902 has a DIVM register that can be used to divide the cclk down. Using DIVM can greatly reduce power when in active mode.

**Problem:**

When DIVM is used in active mode and power-down mode is then entered the P89LPC902 can not be waken up from power-down mode.

**Work-around:**

Before entering power-down mode set DIVM back to 0x00. This way the P89LPC902 will be operating full speed for one instruction before entering power-down mode. After the P89LPC902 has been waken up DIVM can be set back to its original value.

## 4. AC/DC deviations detail

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No known errata

## 5. Errata notes

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### 5.1 $V_{DD}$ .1: $V_{DD}$ power cycling

To generate a proper Power-On Reset (POR),  $V_{DD}$  must have dropped below 0.2 V before being powered back up. Power-cycling without  $V_{DD}$  having dropped below 0.2 V may result in incorrect Program Counter values.

Please also see the  $V_{POR}$  specification in P89LPC902 data sheet, DC electrical characteristics. The Reset section of the data sheet states that during a power cycle,  $V_{DD}$  must fall below  $V_{POR}$ .

### 5.2 IRC.1: Internal RC oscillator accuracy

To be able to guarantee the Internal RC oscillator accuracy over the full operating range the  $V_{DD}$  supply has to be decoupled sufficiently. Sufficient decoupling is dependant on the noise level in the application, typically a 1 uF capacitor should be sufficient for most applications.

Noise on the  $V_{DD}$  supply pins can cause the Internal RC oscillator to go slightly outside of the specified range.

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