

# ERRATA SHEET

**Date:** 2008 Nov 07  
**Document Release:** Version 1.3  
**Device Affected:** P89LPC922

This errata sheet describes both the functional deviations and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

2008 Nov 07

**Identification:**

The typical P89LPC922 devices have the following top-side marking:

P89LPC922x x  
xxxxxxx xx  
xxYYWW R

The last letter in the third line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the P89LPC922:

Revision Identifier (R)	Comment
' - '	Initial device revision
'A'	Second device revision
'B'	Third device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

**Errata Overview - Functional Problems**

Functional Problem	Short Description	fixed in revision	added
DIVM.1	Using DIVM in power-down mode	none	v1.1
I/O.1	Port 3.0 can be an output during a power-up cycle	none	v1.1
ICP.1	ICP Global Erase	A	v1.0
RESET.1	External reset does not function correctly when using DIVM	A	v1.0
UART.1	Breakdetect trips after 10 zero bits	none	v1.1
I/O.2	Eight pins with high drive current can not be driven to 5V in open-drain mode	none	v1.3

**Errata Overview - AC/DC Deviations**

AC/DC Deviation	Short Description	fixed in revision	added
-	-	-	-

**Errata Notes**

Note	Short Description	added
V <sub>DD</sub> .1	V <sub>DD</sub> Power cycling.	v1.1
IRC.1	Internal RC oscillator accuracy	v1.1

## Functional Deviations of P89LPC922

### **DIVM.1: Using DIVM in power-down mode**

- Introduction:** The LPC922 has a DIVM register that can be used to divide the cclk down. Using DIVM can greatly reduce power when in active mode.
- Problem:** When DIVM is used in active mode and power-down mode is then entered the LPC922 can not be waken up from power down mode.
- Workaround:** Before entering powerdown mode set DIVM back to 0x00. This way the LPC922 will be operating full speed for one instruction before entering power-down mode. After the LPC922 has been waken up DIVM can be set back to its original value.

### **I/O.1: Port 3.0 can be an output during a power-up cycle**

- Introduction:** The LPC922 can be selected to be clocked by an internal RC oscillator. When the internal RC oscillator is selected, P3.0 and P3.1 (which would be used for the crystal oscillator circuit) pins can now be used as general purpose IO pins.
- Problem:** When the LPC922 is powered up the configuration of the UCFG1 is read out and the LPC922 configured accordingly. The UCFG1 gets read out on the low brownout level of the LPC922 (typically around 2.3V). Before the UCFG1 is read out the crystal oscillator circuit might be enabled. When the crystal circuit is enabled P3.0 is driven to the inverse state of P3.1.
- Workaround:** Please make sure your external circuitry connected to P3.0 is not affected by this behaviour. Otherwise it is recommended to switch to a different port pin.

### **ICP.1: ICP Global Erase**

- Introduction:** The LPC922 can be programmed using ICP (In Circuit Programming). One of the ICP functions is the Erase Global command, which will erase the entire chip including the security bytes and configuration information.
- Problem:** When giving the Erase Global command through the ICP interface the LPC922 will not clear the busy flag and stay busy forever.
- Workaround:** The workaround can be done in 4 steps:
- Step 1: Shift out the WR\_FMCON command followed by the Erase Global opcode.
  - Step 2: Wait 5ms.
  - Step 3: Do 8 dummy reads with the RD\_FMDATA\_I command.
  - Step 4: Read FMCON until the busy flag gets cleared.

Please also see figure 1 on the following page.

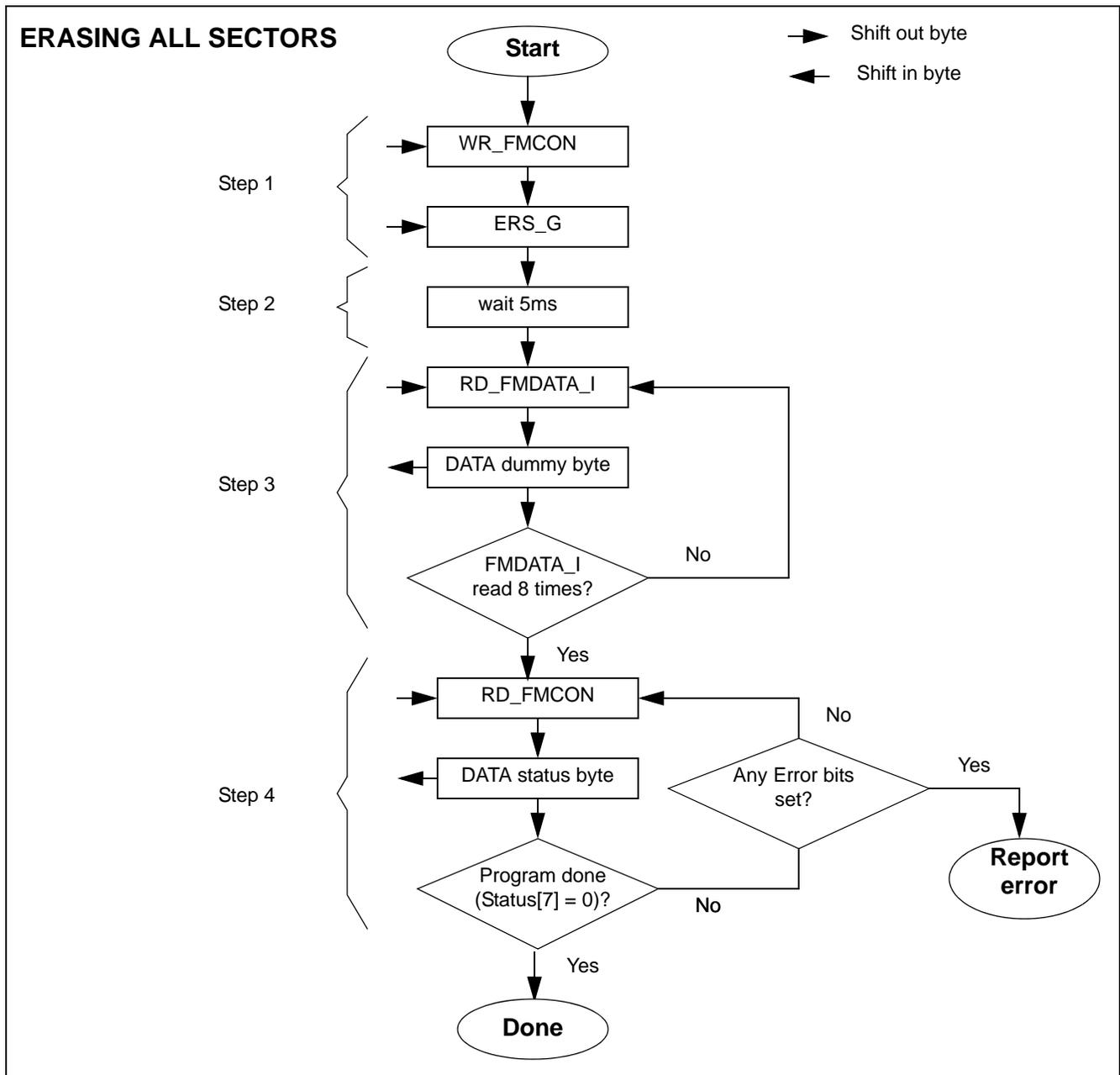


Figure 1: Flowchart ICP Global Erase

**RESET.1: External reset does not function correctly when using DIVM**

**Introduction:** The LPC922 can be set up to use either an internal reset or an external reset pin on P1.5. The DIVM register can be used to divide down the internal CCLK down.

**Problem:** When the LPC922 is configured to have an external reset pin on P1.5 and in the program the DIVM register is programmed to a value different from 0x00 to slow down CCLK, then the next reset pulse will not generate a proper reset for the LPC922. A power cycle has to be applied for the LPC922 to start up again properly.

**Workaround:** Use the internal reset function.

**UART.1: Breakdetect trips after 10 zero bits**

**Introduction:** The UART on the LPC922 has the ability to detect a breakdetect signal, a break signal is a 11 bit long low signal on the RxD input of the UART.

**Problem:** The breakdetect flag will be set after 10 low bits on the RxD input of the UART. When 9 bit mode is used and all 9 data bits are 0 and the start bit is zero this will be detected as a breakdetect.

**Workaround:** No known workaround.

**I/O.2: Eight pins with high drive current can not be driven to 5V in open-drain mode**

**Introduction:** High drive current (20 mA) on eight I/O pins (P0.3 to P0.7, P1.4, P1.6, P1.7). All other port pins have high sinking capability (20 mA).

**Problem:** In open-drain mode, the eight pins with high drive current can not be pulled up to 5V, only can be driven to  $V_{dd}+0.7V$ .

**Workaround:** No known workaround.

## **Electrical and Timing Specification Deviations of P89LPC922**

No known erratas.

## Errata Notes

### **V<sub>DD</sub>.1: V<sub>DD</sub> Power cycling**

To generate a proper Power-On-Reset (POR), V<sub>DD</sub> must have dropped below 0.2V before being powered back up. Power-cycling without V<sub>DD</sub> having dropped below 0.2V may result in incorrect Program Counter values.

Please also see the V<sub>POR</sub> specification in LPC922 Datasheet, DC electrical characteristics. Section 8.15 (Reset) states that during a power cycle, V<sub>DD</sub> must fall below V<sub>POR</sub>.

### **IRC.1: Internal RC oscillator accuracy**

To be able to guarantee the Internal RC oscillator accuracy over the full operating range the V<sub>DD</sub> supply has to be decoupled sufficiently. Sufficient decoupling is dependant on the noise level in the application, typically a 0.1uF should be sufficient for most applications.

Noise on the V<sub>DD</sub> supply pins can cause the Internal RC oscillator to go slightly outside of the specified range.