ES_P89LPC971

Errata sheet P89LPC971

Rev. 2 — 5 October 2010 **Errata sheet**

Document information

Info	Content
Keywords	P89LPC971 errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table at the end of the document.

Revision history

Rev	Date	Description
2	20101005	• Added COMPARATOR.1
1	20100701	• Initial version

Contact information

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1. Product identification

The P89LPC971 devices typically have the following top-side marking:

P89LPC971 x x

xxxxxxx xx

xxYYWW R

The last letter in the last line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the P89LPC971:

Table 1. Device revision table

Revision identifier (R)	Revision description
'-'	Initial device revision
'A'	Second device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
I/O.1	I/O glitch at the beginning of POR	'-', 'A'	Section 3.1 on page 4
WD.1	Possible watchdog reset failure	'-', 'A'	Section 3.2 on page 4
COMPARATOR.1	Possible CMPREF config error	'-', 'A'	Section 3.3 on page 5

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

Table 4. Errata notes table

Errata notes	Short description	Revision identifier	Detailed description
POR.1	Current increase at POR for a couple of seconds	'-', 'A'	Section 5.1 on page 5
Power.1	High leakage current may occur in total power down mode under low temperature	'-', 'A'	Section 5.2 on page 5

3. Functional problems detail

3.1 I/O.1: I/O glitch at the beginning of POR

Introduction:

The I/O pins should be initialized as input-only (PxM1.y = 1, PxM2.y = 0) after internal POR signal is ready.

Problem:

During POR, the I/O glitch happens after power supply >V_{th} and before the internal regulator starts to output current. The glitch occurs on most I/O pins (except P1.2, P1.3 and P1.5). Typical value of V_{th} is 0.7 V.

The width and level of the I/O glitch depend on power supply ramp up rate. For example, when power supply ramps up at 5 V/ms, the I/O glitch is less than 1.8 V and lasts less than 180 μs.

Work-around:

1. Slowing down the power supply ramp up rate can lower down the I/O glitch level and width.
2. Adding a pull-down resistor can reduce I/O glitch level and width. After power up, configure the I/O pin in push-pull mode for I/O pin usage. For example, when power supply ramps up at 3 V/ms, adding a 440 Ω pull-down resistor can reduce the glitch level from 1.8 V to 0.9 V, and width from 180 μs to 100 μs. Please note that this work-around may use more current when the I/O pin outputs ‘1’.
3. Adding pull-up resistor to avoid I/O glitch. After power up, configure the I/O pin in open-drain mode for I/O pin usage.

3.2 WD.1: Possible watchdog reset failure

Introduction:

When watchdog reset occurs, it will reset the chip; its behavior is similar to power on reset. Both POF and BOF are cleared.

Problem:

The watchdog reset might fail in normal or idle mode. Power on reset is needed to reset the chip.

Work-around:

1. WD interrupt plus software reset.
2. Choose the CPU clock as the clock source of watchdog timer to solve the issue. For example, if the CPU uses on-chip IRC as a system clock, the watchdog timer needs to choose PCLK as the clock source to avoid this issue.

3.3 COMPARATOR.1: Possible CMPREF config failure

Introduction:

The user may program one of eight different values for the internal reference voltage using the Comparator Reference register (CMPREF). Each of the two comparators may use a different reference voltage.

Problem:

When the comparator is disabled (CEn bit is zero) and the CMPREF of the same comparator is configured to other values from the default value, the chip may enter into reset state.

Work-around:

Please make sure to enable the comparator (set CEn to one) before configuring the corresponding CMPREF register.

4. AC/DC deviations detail

4.1 n/a

5. Errata notes detail

5.1 POR.1: Current increase at POR for a couple of seconds

Up to 600 μA additional current may occur on P89LPC971 during POR and will drop to zero after a couple of seconds (less than 5 seconds).

5.2 Power.1: High leakage current may occur in total power down mode under low temperature

Under low temperature (0 °C to −40 °C), when entering into total power down mode, P89LPC971 may have high leakage current occured and last from one second to several minutes which depends on the different temperature. During the period, the average current is about 30 μA.

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