This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table.
Table 1. Revision history

<table>
<thead>
<tr>
<th>Rev</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>20200811</td>
<td>• Updated ER101 as per CIN 2020080221</td>
</tr>
<tr>
<td>1</td>
<td>20191127</td>
<td>• Initial release (ER101)</td>
</tr>
</tbody>
</table>
1 Product identification

This errata document applies to PF8100 and PF8200 identified in the following table.

<table>
<thead>
<tr>
<th>Revision ID</th>
<th>Part number</th>
<th>Package</th>
<th>Device marking</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>MC33PF8100xxES (xx represents all OTP versions of this device)</td>
<td>56-pin 8 x 8 mm QFN</td>
<td>MC33PF8100xxES</td>
</tr>
<tr>
<td>C1</td>
<td>MC33PF8200xxES (xx represents all OTP versions of this device)</td>
<td>56-pin 8 x 8 mm QFN</td>
<td>MC33PF8200xxES</td>
</tr>
</tbody>
</table>

1.1 Device build information / date code

The marked trace code is the link between the physically marked materials and the manufacturing lot’s system genealogy information. Once the connection between the marked material and system genealogy information is made, traceability reports provide the material’s manufacturing/shipping history. All devices listed in the errata sheet are affected unless specific date codes are provided.
## 2 Errata overview

<table>
<thead>
<tr>
<th>Erratum ID</th>
<th>Short description</th>
<th>Severity level</th>
<th>Work-around</th>
<th>Product version</th>
<th>Detailed description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ER101</td>
<td>Output overshoot/undershoot when enabling another regulator</td>
<td>Medium</td>
<td>Yes</td>
<td>C1</td>
<td>Section 3.1</td>
</tr>
</tbody>
</table>

[1] High: Failure mode that severely inhibits the use of the device for all or a majority of intended applications  
[2] Medium: Failure mode that might restrict or limit the use of the device for all or a majority of intended applications  
[3] Low: Unexpected behavior that does not cause significant problems for the intended applications of the device  
[4] Enhancement: Improvement made to the device due to previously found issues on the design
3 Functional problems detail

3.1 ER101: Output overshoot/undershoot when enabling another regulator

3.1.1 Severity level
Medium

3.1.2 Problem
Overshoot observed on SW1, SW5 and SW7 when a specific regulator is enabled after the respective switching regulator.

The specific interactions are as follows:
- SW1 is affected, when LDO1 is enabled (aggressor)
- SW5 is affected, when LDO3 is enabled (aggressor)
- SW6 is affected, when SW7 is enabled (aggressor)

When the affected regulator is using the default output capacitance (2 × 44 µF), the overshoot / undershoot can be as high as ±200 mV. The overshoot / undershoot occurs only when the OV/UV monitor of the aggressor is enabled, therefore it can occur during the power-up sequence when the aggressor is turned On at a slot greater than the affected regulator, or during normal operation if the OV/UV monitor of the aggressor is enabled while the affected regulator is already On.
When the affected regulator is configured in dual phase, turning On the aggressor creates a glitch at the output of the affected phase, however, the second phase helps to mitigate the impact causing only around 52 mV (peak to peak) glitch on the regulator output when using the nominal capacitance 4 x 22 µF.

Triple phase and quad phase configurations are not significantly affected by this condition.

3.1.3 Root cause

The PF8x00 uses a centralized bias generation block from which bias signals are routed to the respective blocks. Because of the high-density routing on PF8x00 device, some of the bias traces are too close to each other, causing induced noise to the nearby neighbors.

On production silicon C1, most of the conditions observed on B0 silicon are solved, however, we discovered the following interactions are still present:

- SW5 is affected by the bias trace of the OV/UV monitor of LDO3
- SW1 is affected by the bias trace of the OV/UV monitor of LDO1
- SW6 is affected by the bias trace of the OV/UV monitor of SW7

When the regulator is enabled, the OV/UV monitor is enabled as well, causing the inductive kick on the bias trace of the affected regulator, therefore creating the glitch at the output.
3.1.4 Work-around

1. The overshoot / undershoot is reduced with a higher output capacitance. The systems using PF8x00 PMIC to power the i.MX8 MCUs are already loading the switching regulators from 150 µF to 200 µF. Based on the characterization test, the overshoot / undershoot, gets reduced to a total ~55 mV (peak to peak) with an output capacitance of 150 µF.

![Overshoot/Undershoot Graph](image)

2. Ensure that the aggressor is turned On before or in the same slot as the affected regulator.
   - If all LDOs are not used, avoid using LDO3 if it cannot meet this condition.
   - If all LDOs are not used, avoid using LDO1 if it cannot meet this condition.

3. Do not toggle the aggressor Off and On during normal operation.

3.1.5 Fix plan

No new silicon revision planned.
4 Legal information

4.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

4.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors’ aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer’s sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer’s applications and products planned, as well as for the planned application and use of customer’s third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer’s applications or products, or the application or use by customer’s third party customer(s). Customer is responsible for doing all necessary testing for the customer’s applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer’s third party customer(s). NXP does not accept any liability in this respect.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer’s own risk.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

4.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NXP — is a trademark of NXP B.V.
Contents

1 Product identification ......................................... 3
  1.1 Device build information / date code ................. 3
2 Errata overview ................................................... 4
3 Functional problems detail ................................. 5
  3.1 ER101: Output overshoot/undershoot when enabling another regulator ................. 5
    3.1.1 Severity level ........................................... 5
    3.1.2 Problem .................................................... 5
    3.1.3 Root cause ................................................. 6
    3.1.4 Work-around ............................................ 7
    3.1.5 Fix plan ................................................... 7
4 Legal information ................................................. 8