



Mask Set Errata for Mask 0N89E

This document contains errata information for Kinetis Mask Set 0N89E but excludes any information on security-related modules.

A nondisclosure agreement (NDA) is required for any security-related module information.

For more information on obtaining an NDA, please contact your local Freescale sales representative.

Mask Set Errata for Mask 0N89E

Introduction

This report applies to mask 0N89E for these products:

- KINETIS

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e4588: DMAMUX: When using PIT with "always enabled" request, DMA request does not deassert correctly

Errata type: Errata

Description: The PIT module is not assigned as a stand-alone DMA request source in the DMA request mux. Instead, the PIT is used as the trigger for the DMAMUX periodic trigger mode. If you want to use one of the PIT channels for periodic DMA requests, you would use the periodic trigger mode in conjunction with one of the "always enabled" DMA requests. However, the DMA request does not assert correctly in this case.

Instead of sending a single DMA request every time the PIT expires, the first time the PIT triggers a DMA transfer the "always enabled" source will not negate its request. This results in the DMA request remaining asserted continuously after the first trigger.

Workaround: Use of the PIT to trigger DMA channels where the major loop count is greater than one is not recommended. For periodic triggering of DMA requests with major loop counts greater than one, we recommended using another timer module instead of the PIT.

If using the PIT to trigger a DMA channel where the major loop count is set to one, then in order to get the desired periodic triggering, the DMA must do the following in the interrupt service routine for the DMA_DONE interrupt:

1. Set the DMA_TCDn_CSR[DREQ] bit and configure DMAMUX_CHCFGn[ENBL] = 0
2. Then again DMAMUX_CHCFGn[ENBL] = 1, DMASREQ=channel in your DMA DONE interrupt service routine so that "always enabled" source could negate its request then DMA request could be negated.

This will allow the desired periodic triggering to function as expected.

e5751: FTFx: Launching the Read 1's Section command (RD1SEC) on an entire flash block results in access error (ACCER).

Errata type: Errata

Description: FTFx: Launching the Read 1's Section command on an entire flash block (i.e. with flash address = flash block base address & number of longwords = total number of longwords in the flash block) results in an incorrectly asserted access error (ACCER).

Workaround: To verify an entire flash block, use the Read 1's Block command. Use the Read 1's Section command only to verify sections that are smaller than an entire flash block.

e5706: FTFx: MCU security is inadvertently enabled (secured) if a mass erase is executed when the flash blocks/halves are swapped. This issue only affects applications that use the flash swap feature.

Errata type: Errata

Description: When the logical addresses of the flash blocks (halves) are swapped via the flash swap control command sequence and a mass erase is executed (via the MDM-AP or EzPort), the MCU security can go from un-secure to secure. Thus, when using a debugger to erase the entire flash memory and re-download a software application, the debugger may report that the device is secure after the erase completes. This issue only affects applications that use the flash swap feature.

Workaround: Issue the mass erase request (via the MDM-AP or EzPort) a second time to un-secure the device.

e2793: I2C: MCU does not wake as expected from STOP or VLPS mode on subsequent address matches if previous address is mismatched

Errata type: Errata

Description: The I2C module, acting as a slave on the I2C bus, does not wake as expected from normal STOP mode or VLPS mode on a valid address match if the previous address was not a match.

When the external I2C master sends a non-matching address, the I2C slave state machine does not look for a start bit past the first start bit on the bus. Consequently, subsequent transmissions by the I2C master with a matching address do not, on the first matching address, wake the MCU from stop mode or VLPS via the I2C interrupt.

Workaround: There are multiple workarounds:

(1) The master must continually re-transmit the MCU's slave address upon not receiving a NACK from the slave device during the slave addressing phase of the transmission. For clarification, the master must perform the following:

- a) Send slave device address
- b) Check for ACK bit
- c) If ACK was received, continue with data transmission. Else, send repeated start signal and repeat steps a-c.

NOTE: Due to the nature of the errata, the maximum number of retransmissions needed to wake the part is nine times.

(2) When the MCU, operating as an I2C slave, is in STOP or VLPS mode: Ensure that the external I2C master sends a matching address to wake the slave MCU before it sends any transaction to other I2C slaves. The user must also ensure that MCU does not return to STOP or VLPS until after all packets to non-matching addresses have been sent.

(3) Use a pin interrupt (any pin, whether that pin is or is not being used by the active I2C module) to wake up the part before receiving I2C packets. NOTE: If using the SDA or SCL pin that the active I2C module is using, the part will wake-up on every I2C transaction on the bus.

(4) Use Wait mode instead of STOP or VLPS mode.

e4590: MCG: Transitioning from VLPS to VLPR low power modes while in BLPI clock mode is not supported.

Errata type: Errata

Description: Transitioning from VLPS mode back to VLPR (LPWUI control bit = 0) while using BLPI clock mode only, is not supported. During Fast IRC startup, the output clock frequency may exceed the maximum VLPR operating frequency. This does not apply to the BLPE clock mode.

Workaround: There are two options for workarounds

a) Exit to Run instead of VLPR. Before entering VLPR set the LPWUI bit so that when exiting VLPS mode the MCU exits to RUN mode instead of VLPR mode. With LPWUI set any interrupt will exit VLPR or VLPS back into RUN mode. To minimize the impact of the higher RUN current re-enter VLPR quickly.

or

b) Utilize MCG clock mode BLPE when transitioning from VLPS to VLPR modes.

e4176: NMI: NMI interrupt service routine (ISR) might not be called when MCU wakes up from VLLSx modes.

Errata type: Errata

Description: When MCU wakes up from VLLSx modes via NMI pin the NMI ISR might not be called if the NMI pulse width is lower than 120us..

Workaround: NMI pulse width must be asserted for at least 120usec to ensure NMI ISR is called and entered. Note that a short NMI pulse will still wakeup the part, and the LLWU ISR will still be entered.

e6665: Operating requirements: Limitation of the device operating range

Errata type: Errata

Description: Some devices, when power is applied, may not consistently begin to execute code under certain voltage and temperature conditions. Applications that power up with either VDD \geq 2.0 V or temperature \geq -20C are not impacted. Entry and exit of low-power modes is not impacted.

Workaround: To avoid this unwanted behavior, one or both of these conditions must be met:

a) Perform power on reset of the device with a supply voltage (VDD) equal-to or greater-than 2.0 V , or

b) Perform power on reset of the device at a temperature at or above -20 C.

e6348: PMC: Incorrect reset source indication when waking up from VLLS0 mode.

Errata type: Errata

Description: If MCU exits VLLS0 with the VBAT pin floating and with POR detect circuit enabled (SMC_VLLSCTRL[PORPO] = 0), the MCU may incorrectly indicate tamper detect as a reset source in the RCM_SRS1 register after it wakes up. Under these conditions, the indication of a tamper detect as a false reset source occurs regardless of whether the device features the tamper detection unit (DryIce).

Workaround: Either ensure that VBAT is powered when MCU is exiting VLLS0 mode or disable the POR detect circuit (SMC_VLLSCTRL[PORPO] = 1) before entering VLLS0 mode.

e5666: PMC: Maximum current consumption in VLPR, VLPW, VLPS, LLS and VLLS modes may be higher than data sheet specification.

Errata type: Errata

Description: Maximum current consumption in Very Low Power Run (VLPR), Very Low Power Wait (VLPW), Very Low Power Stop (VLPS), Low Leakage Stop (LLS), Very Low Leakage Stop3 (VLLS3), Very Low Leakage Stop2 (VLLS2), Very Low Leakage Stop1 (VLLS1), and Very Low Leakage Stop0 (VLLS0) modes within an operating range of -40°C to 25°C may exceed data sheet specification.

Note: Some devices do not feature all of the power modes listed above. Refer to the Reference Manual to determine if a particular low power mode is available on your device.

Workaround: If maximum current consumption in these low power modes exceed system requirements, a higher power mode should be used.

e4481: PMC: STOP mode recovery unstable

Errata type: Errata

Description: Recovery from STOP mode is not guaranteed if STOP mode is used for a period of time longer than 50ms.

Workaround: There are two methods that can be used:

1. Set the BGEN bit in the PMC_REGSC register prior to entering STOP mode, and when existing STOP mode clear the BGEN bit.
2. Use a different low power mode such as VLPS.

e4638: PMC: VLLSx mode current draw at cold can exceed maximum specification at cold

Errata type: Errata

Description: When operating below -20C and above 3.4V in a VLLSx mode, current consumption can behave non-linearly and exceed maximum specification at cold. Current draw may approach maximum specification at hot.

Workaround: Limit operating temperature to -20C or greater or keep operating voltage below 3.4V, otherwise design power supply scheme should account for maximum specification as specified for hot.

e5667: PMC: When used as an input to ADC or CMP modules, the PMC bandgap 1-V voltage reference is not available in VLPx, LLS, or VLLSx modes

Errata type: Errata

Description: The Power Management Controller (PMC) bandgap 1-V reference is not available as an input to the Analog-to-Digital Converter (ADC) module (using ADC input channel AD27) or the Comparator (CMP) module (using CMP input IN6) in Very Low Power Run (VLPR), Very Low Power Wait (VLPW), Very Low Power Stop (VLPS), Low Leakage Stop (LLS), Very Low Leakage Stop3 (VLLS3), Very Low Leakage Stop2 (VLLS2), Very Low Leakage Stop1 (VLLS1), or Very Low Leakage Stop0 (VLLS0) modes.

This erratum does not apply to the VREF module 1.2 V reference voltage.

Workaround: Use of the PMC bandgap 1-V reference voltage as an input to the ADC and CMP modules requires the MCU to be in Run, Wait, or Stop modes.

e5138: RTC: The RTC_WAKEUP pin does not operate as specified and the WPON bit in RTC_IER register does not work

Errata type: Errata

Description: This errata only applies to devices that contain the RTC_WAKEUP pin. When an ALARM occurs and this pin is asserted, it is quickly de-asserted when MCU VDD level reaches the POR threshold. In addition, the WPON bit in the RTC_IER register which controls the state of the RTC_WAKEUP pin has no affect, and setting or clearing this bit will not change the state of the RTC_WAKEUP pin.

Only the RTC ALARM interrupt will assert the RTC_WAKEUP pin and a pulse will be generated when the ALARM occurs. If MCU VDD is present the RTC_WAKEUP pin will not remain asserted.

Workaround: For some cases it may be necessary to use an additional GPIO in order to control external circuits. For example, if using an external FET to control MCU VDD, an additional GPIO which asserts is required in order to maintain control of the external FET. This will be corrected on future revisions.

e4949: Reset and Boot: Device may not exit the power on reset (POR) event correctly with fast ramp-up slew rates.

Errata type: Errata

Description: Device may not exit the power on reset (POR) event correctly when the Vdd ramp-up slew rate is greater than 17 kV/sec as VDD is raised from 0V to 1.7V.

Workaround: Keep instantaneous slew rate of VDD below 17 kV/sec.

Status: This errata will be fixed on future mask sets.

e5130: SAI: Under certain conditions, the CPU cannot reenter STOP mode via an asynchronous interrupt wakeup event

Errata type: Errata

Description: If the SAI generates an asynchronous interrupt to wake the core and it attempts to reenter STOP mode, then under certain conditions the STOP mode entry is blocked and the asynchronous interrupt will remain set.

This issue applies to interrupt wakeups due to the FIFO request flags or FIFO warning flags and then only if the time between the STOP mode exit and subsequent STOP mode reentry is less than 3 asynchronous bit clock cycles.

Workaround: Ensure that at least 3 bit clock cycles elapse following an asynchronous interrupt wakeup event, before STOP mode is reentered.

e5472: SMC: Mode transition VLPR->VLLS0(POR disabled)->RUN, will cause POR & LVD.

Errata type: Errata

Description: The Mode transition of VLPR into VLLS0 (POR disabled) then Exit, with LLWU event, back to to RUN mode will cause a POR and LVD reset instead of the expected WAKEUP exit.

Workaround: The recommendation is to transition from VLPR to RUN before entering VLLS0 with POR disabled mode.

e5952: SMC: Wakeup via the LLWU from LLS/VLLS to RUN to VLPR incorrectly triggers an immediate wakeup from the next low power mode entry

Errata type: Errata

Description: Entering VLPR immediately after an LLWU wakeup event from LLS/VLLS, will cause any subsequent entry into LLS/VLLS to fail if entry into VLPR mode occurs before clearing the pending LLWU interrupt.

Workaround: After an LLWU wakeup event from LLS/VLLS, the user must clear the LLWU interrupt prior to entering VLPR mode.

e4647: UART: Flow control timing issue can result in loss of characters if FIFO is not enabled

Errata type: Errata

Description: On UART0 and UART1 when /RTS flow control signal is used in receiver request-to-send mode, the /RTS signal is negated if the number of characters in the Receive FIFO is equal to or greater than the receive watermark. The /RTS signal will not negate until after the last character (the one that makes the condition for /RTS negation true) is completely received and recognized. This creates a delay between the end of the STOP bit and the negation of the /RTS signal. In some cases this delay can be long enough that a transmitter will start transmission of another character before it has a chance to recognize the negation of the /RTS signal (the /CTS input to the transmitter).

Workaround: Always enable the RxFIFO if you are using flow control for UART0 or UART1. The receive watermark should be set to seven or less. This will ensure that there is space for at least one more character in the FIFO when /RTS negates. So in this case no data would be lost.

Note that only UART0 and UART1 are affected. The UARTs that do not have the RxFIFO feature are not affected.

e4945: UART: ISO-7816 T=1 mode receive data format with a single stop bit is not supported

Errata type: Errata

Description: Transmission of ISO-7816 data frames with single stop bit is supported in T=1 mode. Currently in order to receive a frame, two or more stop bits are required. This means that 11 ETU reception based on T=1 protocol is not supported. T=0 protocol is unaffected.

Workaround: Do not send T=1, 11 ETU frames to the UART in ISO-7816 mode. Use 12 ETU transmissions for T=1 protocol instead.

e5704: UART: TC bit in UARTx_S1 register is set before the last character is sent out in ISO7816 T=0 mode

Errata type: Errata

Description: When using the UART in ISO-7816 mode, the UARTx_S1[TC] flag sets after a NACK is received, but before guard time expires.

Workaround: If using the UART in ISO-7816 mode with T=0 and a guard time of 12 ETU, check the UARTn_S1[TC] bit after each byte is transmitted. If a NACK is detected, then the transmitter should be reset.

The recommended code sequence is:

```

UART0_C2 &= ~UART_C2_TE_MASK; //make sure the transmitter is disabled at first
UART0_C3 |= UART_C3_TXDIR_MASK; //set the TX pin as output
UART0_C2 |= UART_C2_TE_MASK; //enable TX
UART0_C2 |= UART_C2_RE_MASK; //enable RX to detect NACK
for(i=0;i<length;i++)
{
while(!(UART0_S1&UART_S1_TDRE_MASK)){}
UART0_D = data[i];
while(!(UART0_S1&UART_S1_TC_MASK)){} //check for NACK
if(UART0_IS7816 & UART_IS7816_TXT_MASK) //check if TXT flag set
{
/* Disable transmit to clear the internal NACK detection counter */
UART0_C2 &= ~UART_C2_TE_MASK;
UART0_IS7816 = UART_IS7816_TXT_MASK; // write one to clear TXT
UART0_C2 |= UART_C2_TE_MASK; // re-enable transmit
}
}
UART0_C2 &= ~UART_C2_TE_MASK; //disable after transmit

```

e5928: USBOTG: USBx_USBTRC0[USBRESET] bit does not operate as expected in all cases

Errata type: Errata

Description: The USBx_USBTRC0[USBRESET] bit is not properly synchronized. In some cases using the bit can cause the USB module to enter an undefined state.

Workaround: Do not use the USBx_USBTRC0[USBRESET] bit. If USB registers need to be written to their reset states, then write those registers manually instead of using the module reset bit.

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