

## Mask Set Errata for Mask 0N32P

This report applies to mask 0N32P for these products:

- MKM34Z256CLQ7
- MKM34Z256CLL7

**Table 1. Errata and Information Summary**

Erratum ID	Erratum Title
e8992	AWIC: Early NMI wakeup not detected upon entry to stop mode from VLPR mode
e10746	In Master-receive mode, the master cannot hold the bus once in the receive phase of the transaction.
e7950	LLWU: When exiting from Low Leakage Stop (LLS) mode using the comparator, the comparator ISR is serviced before the LLWU ISR
e7993	MCG: FLL frequency may be incorrect after changing the FLL reference clock
e7735	MCG: IREFST status bit may set before the IREFS multiplexor switches the FLL reference clock
e6396	sLCD: LCD_GCR[RVTRIM] bits are in reverse order
e9388	The current MPU monitor haddr[16:0] to protect memory is not enough for 256K flash.
e4647	UART: Flow control timing issue can result in loss of characters if FIFO is not enabled

**Table 2. Revision History**

Revision	Changes
18JUN2015	Initial revision
13JAN2017	The following erratum was added. <ul style="list-style-type: none"><li>• e10746</li></ul>



## **e8992: AWIC: Early NMI wakeup not detected upon entry to stop mode from VLPR mode**

**Description:** Upon entry into VLPS from VLPR, if NMI is asserted before the VLPS entry completes, then the NMI does not generate a wakeup to the MCU. However, the NMI interrupt will occur after the MCU wakes up by another wake-up event.

**Workaround:** There are two workarounds:

- 1) First transition from VLPR mode to RUN mode, and then enter into VLPS mode from RUN mode.
- 2) Assert NMI signal for longer than 16 bus clock cycles.

## **e10746: In Master-receive mode, the master cannot hold the bus once in the receive phase of the transaction.**

**Description:** In Master-receive mode, the master cannot hold the bus once in the receive phase of the transaction.

**Workaround:** When configured to receive data, the delay in processing incoming bytes should be minimized. Delay can be minimized by the use of DMA or increased interrupt priority.

## **e7950: LLWU: When exiting from Low Leakage Stop (LLS) mode using the comparator, the comparator ISR is serviced before the LLWU ISR**

**Description:** The comparator's interrupt service routine when exiting from LLS mode is serviced before the LLWU ISR. Clearing the comparator flag in CMPx\_SCR clears the corresponding comparator flag in the LLWU\_Fx register which may be used to determine wakeup source in the LLWU ISR.

**Workaround:** Code can implement a software flag in the CMP ISR to retain wakeup source if required by software.

## **e7993: MCG: FLL frequency may be incorrect after changing the FLL reference clock**

**Description:** When the FLL reference clock is switched between the internal reference clock and the external reference clock, the FLL may jump momentarily or lock at a higher than configured frequency. The higher FLL frequency can affect any peripheral using the FLL clock as its input clock. If the FLL is being used as the system clock source, FLL Engaged Internal (FEI) or FLL Engaged External (FEE), the maximum system clock frequency may be exceeded and can cause indeterminate behavior.

Only transitions from FLL External reference (FBE, FEE) to FLL Internal reference (FBI, FEI) modes and vice versa are affected. Transitions to and from BLPI, BLPE, or PLL clock modes (if supported) are not affected because they disable the FLL. Transitions between the external reference modes or between the internal reference modes are not affected because the reference clock is not changed.

**Workaround:** To prevent the occurrence of this jump in frequency either the MCG\_C4[DMX32] bit must be inverted or the MCG\_C4[DRST\_DRS] bits must be modified to a different value immediately before the change in reference clock is made and then restored back to their original value after the MCG\_S[IREFST] bit reflects the selected reference clock.

If you want to change the MCG\_C4[DMX32] or MCG\_C4[DRST\_DRS] to new values along with the reference clock, the sequence described above must be performed before setting these values to the new value(s).

### **e7735: MCG: IREFST status bit may set before the IREFS multiplexor switches the FLL reference clock**

**Description:** When transitioning from MCG clock modes FBE or FEE to either FBI or FEI, the MCG\_S[IREFST] bit will set to 1 before the IREFS clock multiplexor has actually selected the slow IRC as the reference clock. The delay before the multiplexor actually switches is:

2 cycles of the slow IRC + 2 cycles of OSCERCLK

In the majority of cases this has no effect on the operation of the device.

**Workaround:** In the majority of applications no workaround is required. If there is a requirement to know when the IREFS clock multiplexor has actually switched, and OSCERCLK is no longer being used by the FLL, then wait the equivalent time of:

2 cycles of the slow IRC + 2 cycles of OSCERCLK

after MCG\_S[IREFST] has been set to 1.

### **e6396: sLCD: LCD\_GCR[RVTRIM] bits are in reverse order**

**Description:** The four bits of LCD\_GCR[RVTRIM] are in reverse order, in such a way that the LSB corresponds to bit 27 and the MSB corresponds to bit 24 of the LCD\_GCR. The RVTRIM adjustment from lower voltage to higher voltage does not follow a linear increase in the LCD\_GCR[RVTRIM] value. The RVTRIM adjustment should follow this sequence:

0,8,4,12,2,10,6,14,1,9,5,13,3,7,11,15

to achieve a linear increase from lower voltage to higher voltage.

The reset value of this field is still 8, which corresponds to a low voltage value of the VIREG.

**Workaround:** You can use a lookup table with the correct order of RVTRIM values for a linear change on the VIREG voltage (contrast). If planning to use a user-selectable contrast, a memory buffer is required to keep track of the logic value of the RVTRIM. When required to increase or decrease the contrast of the LCD, the buffer pointer should be increased or decreased accordingly and the corresponding value from the lookup table should be written to the LCD\_GCR[RVTRIM].

To avoid a low voltage on VIREG after reset, LCD\_GCR[RVTRIM] must be updated during the LCD initialization routine.

**e9388: The current MPU monitor haddr[16:0] to protect memory is not enough for 256K flash.**

**Description:** Current MPU monitor haddr[16:0] to protect memory. It is not enough for 256K flash.

**Workaround:** Split and allocate the protected/unprotected code into two sections. The protected code is placed into the lower flash. The unprotected code is placed into the upper flash. The linker script of the chip in the IDE is modified accordingly.

**e4647: UART: Flow control timing issue can result in loss of characters if FIFO is not enabled**

**Description:** On UARTx modules with FIFO depths greater than 1, when the /RTS flow control signal is used in receiver request-to-send mode, the /RTS signal is negated if the number of characters in the Receive FIFO is equal to or greater than the receive watermark. The /RTS signal will not negate until after the last character (the one that makes the condition for /RTS negation true) is completely received and recognized. This creates a delay between the end of the STOP bit and the negation of the /RTS signal. In some cases this delay can be long enough that a transmitter will start transmission of another character before it has a chance to recognize the negation of the /RTS signal (the /CTS input to the transmitter).

**Workaround:** Always enable the RxFIFO if you are using flow control for UARTx modules with FIFO depths greater than 1. The receive watermark should be set to seven or less. This will ensure that there is space for at least one more character in the FIFO when /RTS negates. So in this case no data would be lost.

Note that only UARTx modules with FIFO depths greater than 1 are affected. The UARTs that do not have the RxFIFO feature are not affected. Check the Reference Manual for your device to determine the FIFO depths that are implemented on the UARTx modules for your device.

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