Mask Set Errata for Mask 0N01P

This report applies to mask 0N01P for these products:

- MKL13Z32Vxx4, MKL13Z64Vxx4
- MKL33Z32Vxx4, MKL33Z64Vxx4

Table 1. Errata and Information Summary

Erratum ID	Erratum Title
e3863	ADC: In 16-bit differential mode, ADC may result in a conversion error when positive input is near upper rail reference voltage
e8992	AWIC: Early NMI wakeup not detected upon entry to stop mode from VLPR mode
e6396	sLCD: LCD_GCR[RVTRIM] bits are in reverse order
e2580	UART: Start bit sampling not compliant with LIN 2.1 specification

Table 2. Revision History

Revision	Changes
13 Apr 2015	Initial Release

e3863: ADC: In 16-bit differential mode, ADC may result in a conversion error when positive input is near upper rail reference voltage

Description: In 16-bit differential mode, the ADC may result in a conversion error when the input voltage on the plus-side of the differential pair (DPx) exceeds approximately (VREFH*31/32). Other modes are unaffected.

Workaround: To avoid a conversion error near positive full-scale in this mode, do not allow the input voltage on the plus-side of the differential pair (DPx) to exceed (VREFH*31/32).

e8992: AWIC: Early NMI wakeup not detected upon entry to stop mode from VLPR mode

Description: Upon entry into VLPS from VLPR, if NMI is asserted before the VLPS entry completes, then the NMI does not generate a wakeup to the MCU. However, the NMI interrupt will occur after the MCU wakes up by another wake-up event.

Workaround: There are two workarounds:

1) First transition from VLPR mode to RUN mode, and then enter into VLPS mode from RUN mode.

2) Assert NMI signal for longer than 16 bus clock cycles.

e6396: sLCD: LCD_GCR[RVTRIM] bits are in reverse order

Description: The four bits of LCD_GCR[RVTRIM] are in reverse order, in such a way that the LSB corresponds to bit 27 and the MSB corresponds to bit 24 of the LCD_GCR. The RVTRIM adjustment from lower voltage to higher voltage does not follow a linear increase in the LCD_GCR[RVTRIM] value. The RVTRIM adjustment should follow this sequence:

0,8,4,12,2,10,6,14,1,9,5,13,3,7,11,15

to achieve a linear increase from lower voltage to higher voltage.

The reset value of this field is still 8, which corresponds to a low voltage value of the VIREG.

Workaround: You can use a lookup table with the correct order of RVTRIM values for a linear change on the VIREG voltage (contrast). If planning to use a user-selectable contrast, a memory buffer is required to keep track of the logic value of the RVTRIM. When required to increase or decrease the contrast of the LCD, the buffer pointer should be increased or decreased accordingly and the corresponding value from the lookup table should be written to the LCD_GCR[RVTRIM].

To avoid a low voltage on VIREG after reset, LCD_GCR[RVTRIM] must be updated during the LCD initialization routine.

e2580: UART: Start bit sampling not compliant with LIN 2.1 specification

Description: The LIN 2.1 specification states that start bits should be checked at sample 7, 8, 9, and 10. The UART module checks the start bit at samples 3, 5, and 7 instead.

Workaround: Start bits longer than 5/16 of a bit time are guaranteed to be recognized. Start bits shorter than this should not be used with this version of the UART because they might not be recognized.

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