LS1088A RDB Errata

LS1088A RDB

Errata

Version 15

This document details all known board errata for the LS1088A RDB.

Table 1: Document revision history

Revision	Date	Significant changes
1	2016_0115	Initial Release
2	2016_0119	Fixed E1 picture; E4 values and caps changed; added E6.
3	2016_0121	Added E-00007
4	2016_0212	Added E-00008
5	2016_0329	Updated E-00004 with latest LTC recommendations.
6	2016_0331	Added E-00009
7	2016_0713	Updated E-00007, Added E-00010
8	2016_0822	Added E-00011
9	2016_1109	Added E-00012
10	2016_1219	Added E-00013
11	2017_0620	Added E-00014
12	2017_1127	Added E-00015
13	2017_1204	Added E-00016
14	2018_0724	Added E-00017
15	2018_0808	Added E-00018

Table 2 below summarizes all known errata and lists the corresponding board and schematic revision level to which they apply.

Table 2: Summary of Board Errata and Applicable Revision

Errata	Name	Projected Solution	PCB Revision	Schematic Revision
E-00001	Hardware cannot select DDR4 mode when interposer (LS1043) used.	Convert config to a pulldown.	A	A
E-00002	WiFi Cards May Short Power Rails.	Change pin 24 (2x) to 3V3.	A	A
E-00003	LTC3882 at wrong I2C address.	Change resistors	A	A
E-00004	LTC3882 components are non-optimized.	Optimize performance.	A	A
E-00005	LTC3882 programming header missing.	Install.	A	A
E-00006	No clocks on miniPCIe with certain adapters.	Convert CLKREQ# pullups to pulldowns.	A	A
E-00007	SPI Emulator connector incorrect	Cut key, install rotated.	A, B	A, B
E-00008	TA_BB_RTC not supported.	None.	A	A
E-00009	TA_BB must follow VDD	Do not change VDD.	A	A
E-00010	JTAG Header shorted	Wire around JTAG mux.	B	B
E-00011	PCIE Slot clock always runs.	None.	B,C	B,C

E-00012	Rotation Detect does not work.	None.	A,B,C	A,B,C
E-00013	TDM does not work	Wire around mux	A,B,C	A,B,C
E-00014	SVDD switch notes incorrect	None.	A,B,C	A,B,C
E-00015	TDM requires no pullups	Remove resistors.	A,B,C	A,B,C
E-00016	SDHC CD/WP incorrect.	CPLD Update.	Any	n/a
E-00017	SDHC CD/WP erratic if not in chassis	Use chassis or add resistor.	A,B,C,D	A,B,C,D
E-00018	USB1/USB2 front panel labels	Apply overlay	B,C,D	B,C,D

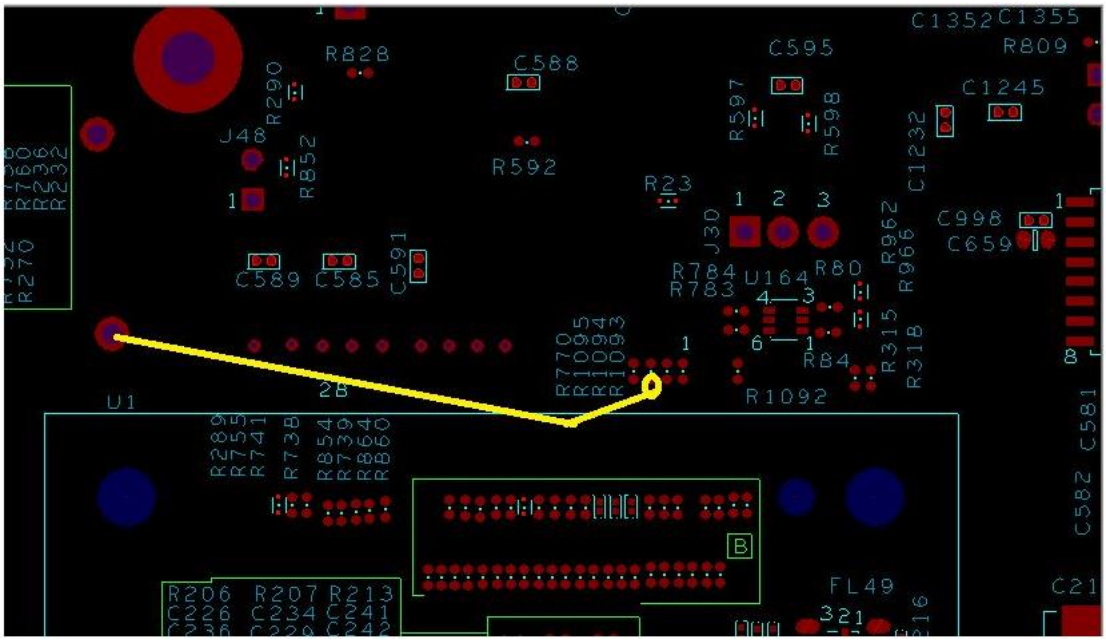
E-00001: DDR4 Selection for Interposer (LS1043A)

Description: LS1043A requires “cfg_dram_type=0” to select DDR4, the opposite that of the LS1088.

Impact: DDR will not work.

Workaround: Convert R1095 from a pullup to a pulldown.

1. Remove R1095, reinstall with pin 1 on the bottom pad and pin 2 free.
2. Connect R1095 pin 2 to ground at location shown.



Fix: All Rev A boards have had the above rework instructions applied.
A permanent fix will be done on PCB Rev. B where the CPLD will drive the correct value based on the device type used (LS1043 or LS1088).

Note: This rework must be reverted if the LS1088A is installed.

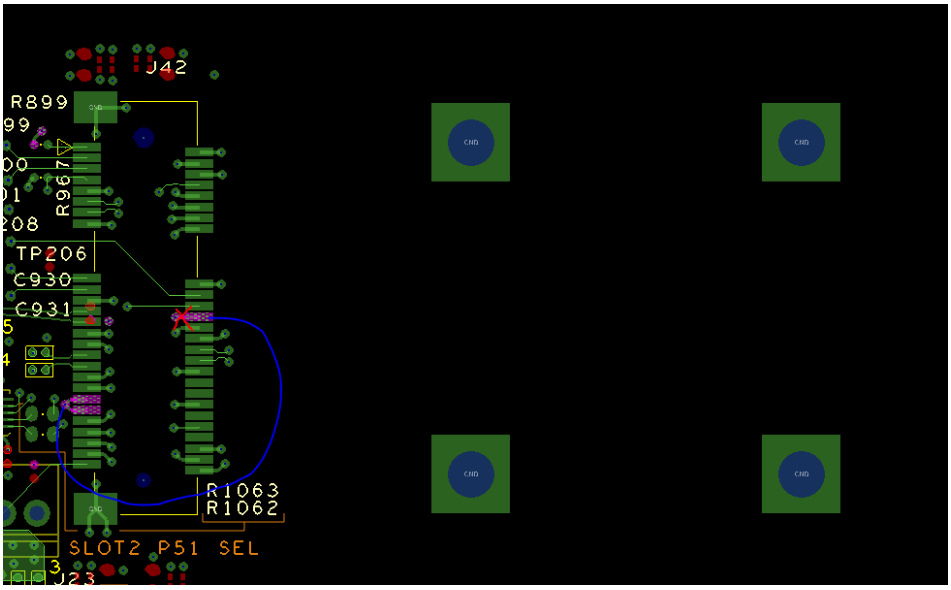
E-00002: **WiFi Cards May Short Power Rails.**

Description: Certain WiFi cards connect 3V3SB and 3V3.

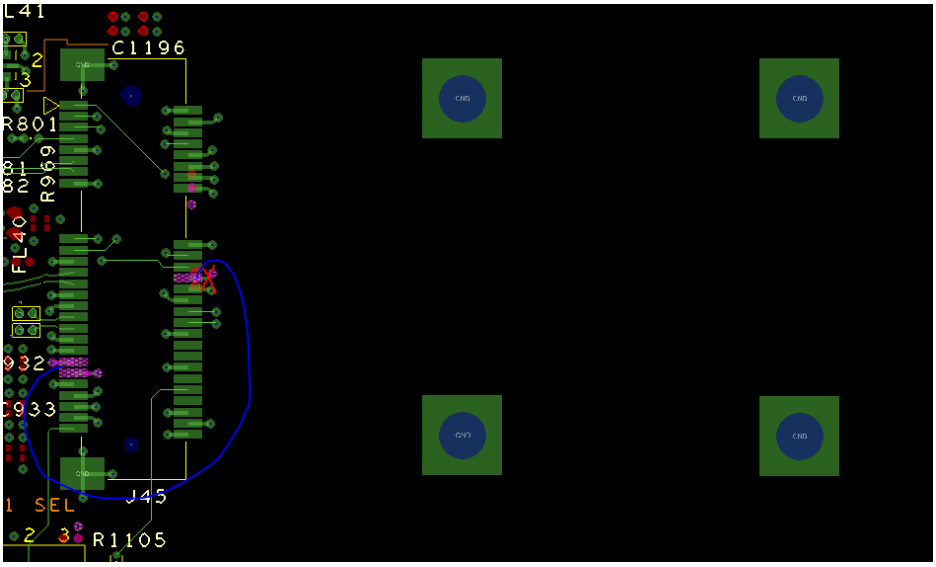
Impact: Installing such cards causes the system to incorrectly power-on.

Workaround: Modify J42 and J45 as follows:

1. Cut trace between pad and via at J42 pin 24 (BEFORE ASSEMBLY) –or – Lift J42 pin 24 and isolate from pad with Kapton tape (AFTER ASSEMBLY).
2. Wire from J42 pin 24 to J42 pin 39/41 (shown in blue).



3. Cut trace from J45 pin 24 to via (red X).
4. Wire from J45 pin 24 to J45 pin 39/41 (shown in blue).



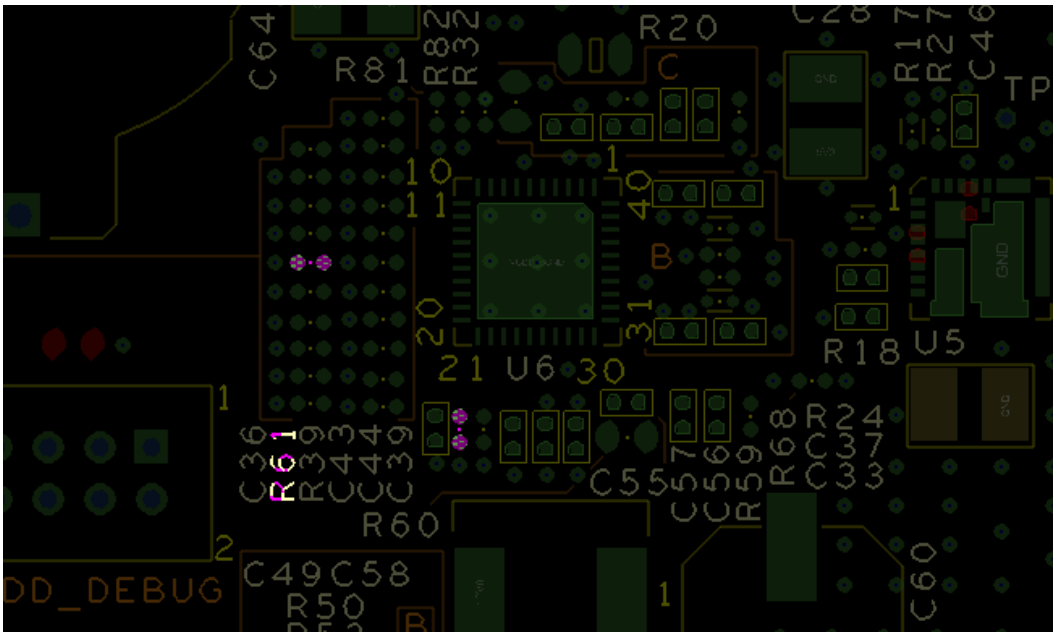
Fix: All Rev A boards have had the above rework instructions applied. Will be fixed on PCB Rev. B.

E-00003: LTC3882 at incorrect I2C address.

Description: The LTC3882 I2C (PMBus) address should be 0x63. It is currently at 0x66 and cannot be accessed due to the CPLD I2C address (0x66).

Impact: Processor cannot access LTC3882 for PMBus VDD setup, or monitoring.

Workaround: 1. Change R69 to 4.32K
2. Change R61 to 10K.



Fix: All Rev A boards have had the above rework instructions applied.
Will be fixed on schematic Rev A1 and PCB Rev. B.

E-00004: LTC3882 Components are non-optimized.

Description: LTC3882 schematic uses non-optimized components.

Impact: Performance is adequate but may exhibit issues under high-performance demands.

Workaround: Change components as follows:

Component	Was	Change To
R58	10.7k	3.48k 1%
C54	470pF	330pF
C50	470pF	1000pF
C53	5pF	10pF
R56	52.3k	30.1k 1%
R59	6.34k	3.48k 1%
C56	470pF	330pF
C55	2pF	10pF
R60	102k	30.1k 1%
C57	220pF	1000pF

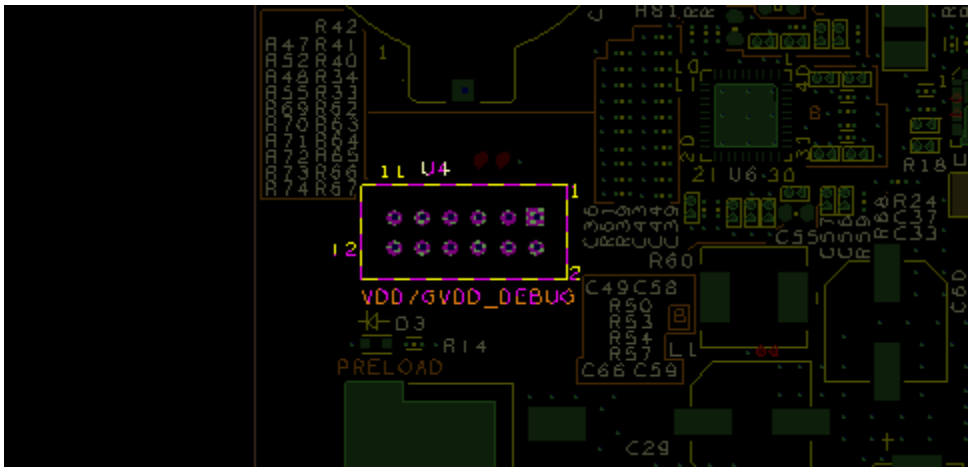
Fix: All Rev A boards have had the above rework instructions applied.
Will be fixed on schematics rev A1 or later.

E-00005: **LTC3882 Programming Header Missing**

Description: U4 is required.

Impact: U4 is required for assembly and test.

Workaround: Install U4 (FCI #98414-G08-12ULF, Agile P/N 210-80051).



Fix: All Rev A boards have had the above rework instructions applied.
Will be fixed on schematics rev A1 or later.

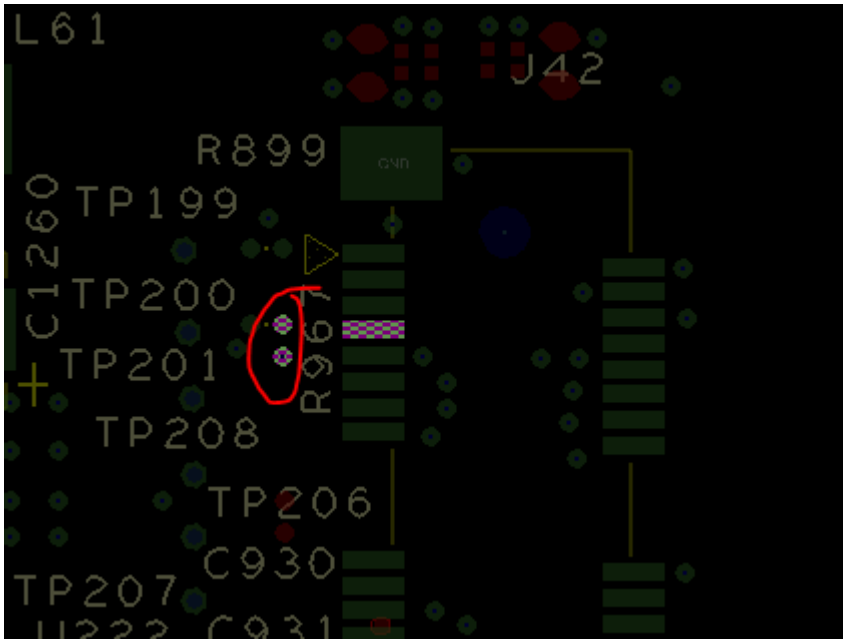
E-00006: **No clocks on miniPCIe with Certain Adapters**

Description: Using some miniPCIe-to-PCIe adapters may not work as CLKREQ# is not asserted.

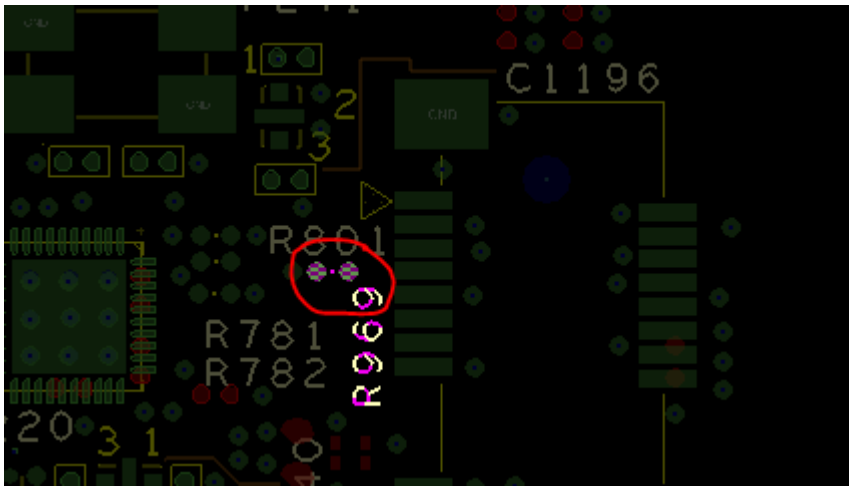
Impact: PCIe cards in an adapter are not usable.

Workaround: The clock driver has internal pulldowns; removing the pullups will all the clocks to always run.

1. Remove R967.



3. Remove R969.



Fix: All Rev A boards have had the above rework instructions applied.
Will be fixed on schematics rev A1 or later.

E-00007: **QSPI Emulator Header is Incorrect**

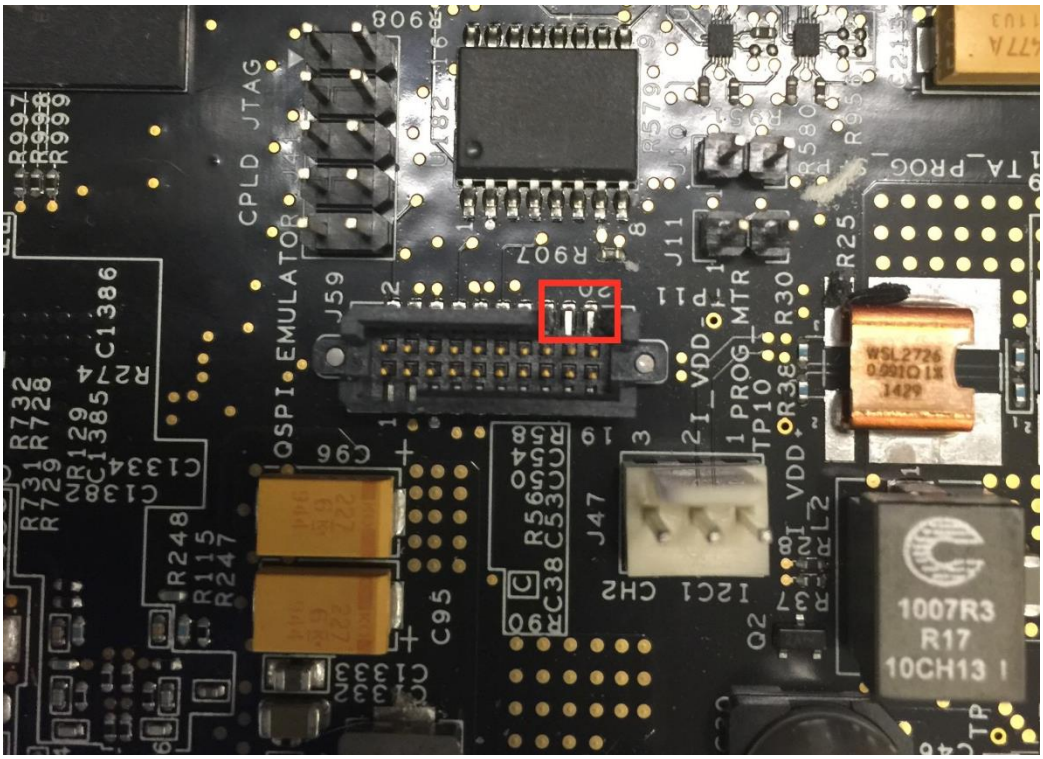
Description: The pinout of J59 does not match the DediProj QSPI emulator

Impact: Emulator is not usable.

Workaround: Pin 1 should be diagonally opposite the alignment key. There are two possible workarounds:

1. Remove J59 and reinstall rotated 180 degrees. If possible, rotate prior to board assembly.

2. Use cutters to remove part of the sidewall of J59. The width should be two pins worth:



Fix: Install the part such that the mechanical key is opposite pin 1.
Note: schematics and boards are all correct, this is an assembly issue.

E-00008: TA_BB_RTC not Supported

Description: The LS1043/LS1088 silicon does not support TA_BB_RTC. The pin should be ground/0V.

Impact: Damage may occur on future silicon revs when the device pin becomes ground.

Workaround: J30 should have a jumper between pins 1 and 2, and this should not be removed or changed.

Fix: All Rev A boards are shipped with J30 shorted between pins 1 and 2.
Will be fixed on PCB rev B or later.

E-00009: TA_BB must track VDD

Description: There is no provision to alter TA_BB if software adjusts VDD based on fuse settings.

Impact: Damage may occur to silicon if TA_BB is set to 0.9V and VDD is set to 1.0V, or vice-versa.

Workaround: Set TA_BB jumper to 1.0V and do not change.
Query the PCB revision in the QixMin (CPLD) registers: if Rev A, do not change VDD (via PMBus) no matter what the fuses recommend.

Fix: All Rev A boards are shipped with TA_BB set to 1.0V.
Rev B boards will introduce a register bit that allows TA_BB to change between 0.9V and 1.0V. Software can use this bit to alter TA_BB when it changes VDD.

E-00010: JTAG Header Shorted

Description: A schematic net is misplaced, causing all even JTAG header pins to be shorted.

Impact: JTAG is unusable; processor will not exit reset.

Workaround: 1.) Remove J55. Isolate pins 2, 4, 6, 8, and 10. Reattach J55 and secure with epoxy as needed.

2.) Remove R290.

3.) Perform the following mods, routing wires through the BH8 Mounting Hole:

3a. Connect J55 pin 2 (JTAG_TMS_CON) to R835, pin 2 (DUT_TMS)

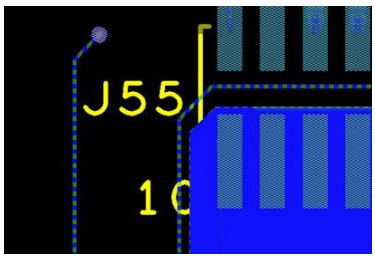
3b. Connect J55 pin 4 (JTAG_TCK_CON) to R855, pin 2 (DUT_TCK)

3c. Connect J55 pin 6 (JTAG_TDO_CON) to R854, pin 2 (DUT_TDO)

3d. Connect J55 pin 8 (JTAG_TDI_CON) to R853, pin 2 (DUT_TDI)

3e. Connect J55 pin 1 (OVDD) through a 100 ohm resistor to OVDD at R739, pin 1. Secure the 100 ohm resistor to the PCB using epoxy as needed.

3f. Connect J55 pin 10 (JTAG_RST_B) to nearby via (above letter J in J55):



4.) Install shorting header at J48, pins 1 and 2.

Note that with this rework, J48 functions as follows:

SHORTED	- JTAG header connect to processor.
OPEN	- CPLD can be programmed via J41

Fix: Move misplaced schematic net to eliminate short.

E-00011: PCIE Slot Clock Always Runs

Description: The internal CPLD pullup is not sufficient to pull PRESENT_SLOT3_B high and disable the slot clock when no card is installed.

Impact: SLOT3 always shows a card is installed in the STAT_PRES2 register.
Possibly slightly more EMI emissions.

Workaround: Do not rely on STAT_PRES2[5] in software.

Fix: None**,** due to low impact.

E-00012: Rotation Detect not Supported

Description: The LS1088 silicon does not support rotation detection, therefore the LS1088ARDB detection circuitry cannot work.

Impact: If the CPU is inserted into the CPU socket incorrectly (mis-oriented), the "ROT_ERR" LED will not illuminate, and the board will be allowed to power on. A power up of the CPU with it incorrectly installed in the socket will likely cause damage to the CPU, the socket and the PCB.

Workaround: None.

Fix: None. Systems are now shipped with soldered-down CPUs, so the impact is minimal.

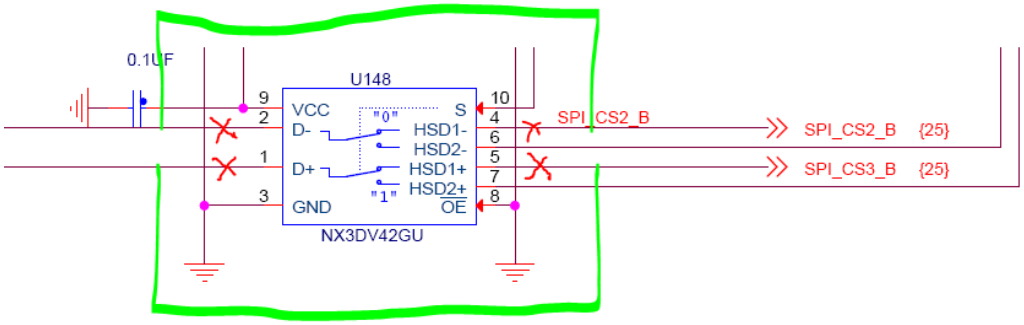
E-00013: **TDM Slot Not Working**

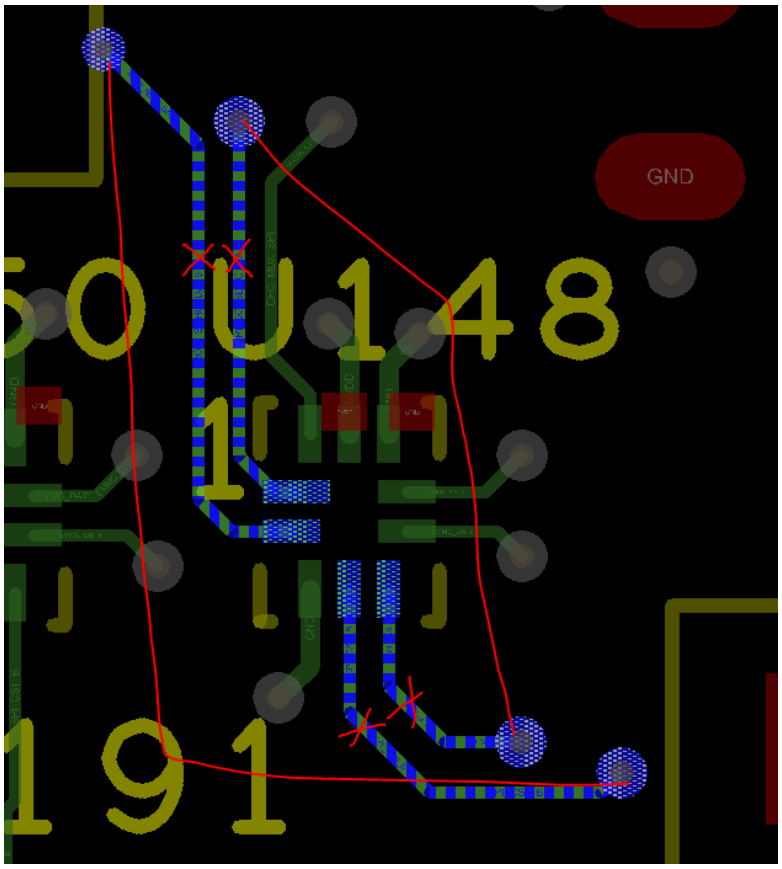
Description: The two SPI chip selects used for TDM (SPI_CS2_B and SPI_CS3_B) pass through a mux with sufficient series resistance to cause issues in the weak-drive voltage translation devices (NTB0104BQ). The CS signals oscillate, or remain in the previous drive level.

Impact: The TDM Riser card will not work.

Workaround: **NOTE**: This workaround will disable use of the on-board eMMC device.

The workaround requires wiring across the CS pins that were muxed in U148:





Fix: Since TDM only works on systems which must be opened (and the PCIe riser adapter removed), the optimal solution is to use two 1x3 “berg” headers for zero resistance.

E-00014: Incorrect SVDD Switch Documentation

Description: The schematics show an incorrect SVDD voltage selection. The correct settings are:

```
SW_SVDD_SEL
==========================================
>> 0 : SVDD defaults to 1.0V
   1 : SVDD defaults to 0.9V
```

Impact: Incorrect SVDD voltage might be selected.

Workaround: Set SW3[4] as required.

Fix: None.

E-00015: TDM Operation Requires no Pullups.

Description: TDM signals expect undriven signals to be low, so pullups for IRQ signals which function as TDM signals must be removed.

Impact: TDM communications do not work.

Workaround: Remove resistors R744-R751.

Fix: Corrected on Rev C1 or later.

E-00016: CD_B/WP signals between CPLD and DUT Crossed.

Description: SDHC CD_B/WP signals reported from slot to LS1088 through the CPLD are crossed over.

Impact: SDHC may not work unless WP is 0 (off), since it incorrectly drives CD_B low to indicate a card is present.

Workaround: Use V1.12 or later CPLD images.

Fix: No impact to any hardware.

E-00017: CD_B/WP signals erratic if board not in chassis.

Description: SDHC CD_B/WP signals report high if board is not in a chassis, regardless of card presence or write protect. The schematic component implies S[1:4] are shields but in fact they are the grounds for CD/WP.

Impact: SDHC may not work unless the board is installed in a chassis.

Workaround: Either:

1. Keep the board in a chassis for SDHC operations.
2. Solder a wire between CGND and GND. The easiest location is P1 (UART stack) mounting holes to TP222 (GND).

Fix: No plans to fix.

E-00018: USB1/USB2 Front Panel Labels are Reversed.

Description: The front panel labels on the chassis describe the vertical USB Type A connector as USB1, and the horizontal USB 3.0 connector as USB2. These are reversed.

Impact: Connected devices will appear on a different USB controller than may be expected. Since linux automounts most devices this may not be easily noticeable except under test conditions.

Workaround: Apply a label to the front panel to relabel the ports:

Incorrect:

Correct:

Fix: No plans to fix.

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