Freescale Semiconductor
Chip Errata

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Rev. 2.3, 10/2006

MC13191

2.4 GHz Low Power Transceiver

1 Introduction

These errata pertains to MC13191 V2.3 engineering samples and later production devices which have been shipped with date code marking 4442 or later. The related IC Data Sheet, MC13191DS, and Reference Manual, MC13191RM apply to these devices. This document is included in shipments for which this errata applies.

2 Updated Errata 08/2006

In addition to the errata described in Section 3, “Revision 2.3 Errata”, the errata described in Table 1 also applies.

Table 1. Errata Update 08/2006 Details

No	Errata	Work Around
1	The Doze current (no CLKO output active) is specified as 35 µA (typical) on the data sheet with the programmed CLKO frequency at a default of 32.786 kHz. This Doze current can be considerably higher for certain combinations of higher CLKO frequencies and event timer prescale options. These combinations consist of: a) CLKO freq = 16 MHZ with prescale select at 5, 6, or 7. b) CLKO freq = 8 MHZ with prescale select at 6, or 7. c) CLKO freq = 4 MHZ with prescale select at 7. All other combinations have no problems. The higher current will not occur every time Doze is enabled. There is no potential harm either to the transceiver or its operation. The Doze current is simply higher.	To work around this issue, there are three choices: a) Accept higher current in Doze mode. b) Do not use any of the described combinations in Doze mode. c) If a higher CLKO frequency is desired when using CLKO as an MCU clock source, and the desired prescale select can cause a problem, just before entering Doze mode, program the CLKO frequency to a lower value. Next, use the desired prescale value while in Doze. Finally, after exiting Doze mode, reprogram CLKO to the desired frequency before releasing the MCU clock to the CLKO source.
2	Asserting ATTN early can cause a problem if the transceiver has not fully entered Hibernate or Doze mode. Once the transceiver has been programmed to enter either Hibernate or Doze, the device does not fully enter the low power mode until 128 CLKO cycles have transpired. This is true whether or not the CLKO output is enabled. If the CLKO delay time is still active and ATTN is asserted, the IRQ for exiting the low power mode will be asserted, but reading the IRQ_Status register during the interrupt service routine will return no active bits. The status bit for exiting low power mode will not be set. This above situation can cause a problem with the interrupt service routine if the service routine does not return an interrupt source. The delay time can vary from 128 clock cycles @ 16.393 kHz or ~7.8 msec to 128 clock cycles @ 16 MHz or 8 µsec. This is dependent on the select CLKO frequency	To work around this issue, there are three choices: a) Prevent the application from asserting ATTN during this period. As an example, for an End Node that is sleeping for long periods, this would present no problems. b) If there is a potential for an early transceiver wake-up, program CLKO to a high frequency before entering Hibernate or Doze. The software can prevent an early wake-up within the short 8 µsec time. If this approach is used, the errata described in No 1 must also be considered. c) Write the application software knowing that an interrupt from exiting low power mode may not generate a valid status bit.

3 Revision 2.3 Errata

Table 2. Revision 2.3 Errata Details

No	Errata	Work Around
1	If a new interrupt event occurs during the processing of an existing interrupt, the new event may be lost. If the new interrupt event happens while the IRQ_Status Register 24 is being read ($\overline{CE}$ is asserted), the event status bit may not be set and the $\overline{IRQ}$ output will not stay asserted.	The application workaround is to use Freescale 802.15.4 software Version 1.051 or later, or to use Freescale SMAC Release 4.1 or later. For customers developing custom driver software, the second missing interrupt needs to be handled.
2	Some control bits do not default at reset to required values for best operation.	As part of the initialization procedure after a reset, there are mandatory register bits that must be written: 1. Register 0x08, Bit 1 set to 1. 2. Register 0x08, Bit 4 set to 1. 3. Register 0x11, Bits[9:8] set to 00. 4. Register 0x06, Bit 14 set to 1. The Freescale SMAC software incorporates these writes.

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