

Freescale Semiconductor Chip Errata Document Number: MC1321xCE Rev. 1.4, 05/2009

## MC1321x ZigBee<sup>™</sup>- Compliant Platform - 2.4 GHz Low Power Transceiver for the IEEE<sup>®</sup> 802.15.4 Standard plus Microcontroller

### 1 Introduction

This errata pertains to MC1321x product. This document is included in shipments for which this errata applies. These errata pertain to devices which have been shipped with marking "MC1321x" and date code marking 0920 or later.

- The MC1321x uses the same MCU as the MC9S08GB/GTXXA family and the errata for that device applies to the MCU on the MC1321x.
- The latest MC1321x uses an updated version of the 689S08A 8-bit microprocessor to correct errata associated with the onboard FLL and reset pin.

# 2 HC9S08A Errata

The 689S08A 8-bit CPU on the MC1321x is the MSE9S08GB60A\_4L11Y version die. Please refer to the associated errata for this device, *Document Number MSE9S08GB60A\_4L11Y*, on the Freescale web site.

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IEEE 802.15.4 Transceiver Errata

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The transceiver on the MC1321x is a separate die. The errata described in Table 1 applies.

### Table 1. MC1321x Transceiver Errata

No	Errata	Work Around
1	The Doze current (no CLKO output active) is specified as 35 $\mu$ A (typical) on the data sheet with the programmed CLKO frequency at a default of 32.786 kHz. <u>This Doze current can be considerably higher for certain combinations of higher</u>	To work around this issue, there are three choices: a) Accept higher current in Doze mode.
	<u>CLKO frequencies and event timer prescale options</u> . These combinations consist of:	b) Do not use any of the described combinations in Doze mode.
	<ul> <li>a) CLKO freq = 16 MHZ with prescale select at 5, 6, or 7.</li> <li>b) CLKO freq = 8 MHZ with prescale select at 6, or 7.</li> <li>c) CLKO freq = 4 MHZ with prescale select at 7.</li> <li>All other combinations have no problems. The higher current will not occur every time Doze is enabled. There is no potential harm either to the transceiver or its operation. The Doze current is simply higher.</li> </ul>	c) If a higher CLKO frequency is desired when using CLKO as an MCU clock source, and the desired prescale select can cause a problem, just before entering Doze mode, program the CLKO frequency to a lower value. Next, use the desired prescale value while in Doze. Finally, after exiting Doze mode, reprogram CLKO to the desired frequency before releasing the MCU clock to the CLKO source.
2	Timer Comparator 3 can abort an RX sequence - If an RX sequence (Packet Mode or Streaming Mode) is active and Timer Comp 3 matches the value of the Event Timer "current time" counter, the RX sequence will be aborted. No status bit is set and no interrupt can be generated. Exit from RX mode can only be detected by using GPIO1 as an "out-of-idle" indicator.	<ul> <li>For users writing their own application:</li> <li>a) Never let the counter reach the compare value in Time Comp 3 register.</li> <li>b) Enable Timer Compare 3 always to generate an interrupt. If the interrupt occurs and the RX state was enabled. Take appropriate action, such as restarting RX.</li> </ul>
	Freescale's IEEE 802.15.4 MAC and by inference all associated network stacks compensate for this situation. If users are writing their own software (such as using SMAC),	c) Monitor the "out-of_idle" indicator while in RX mode.
	this condition should be compensated for.	
3	For proper performance of the radio the following <u>modem</u> registers must be over-programmed as shown below:	<ul><li>Write Register 0x31 to 0xA0C0</li><li>Write Register 0x34 to 0xFEC6</li></ul>
	<ul><li>Write Register 0x31 to 0xA0C0</li><li>Write Register 0x34 to 0xFEC6</li></ul>	
	Software can confirm the transceiver version that requires the register over-writes by reading the modem SPI Chip-ID Register, Address 0x2C. Register 0x2C reads as 0x6800 for this device.	



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Document Number: MC1321xCE Rev. 1.4 05/2009

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