

# MC145574 Mask Set G20R1

## Device Errata

This version of the MC145574 silicon has BR15 mask code = \$11. This errata sheet applies to devices having mask set G20R1.

## Problem:

In NT Terminal mode (mode used in the Smart NT1 application), when the MC145574 is not activated (it transmits Info0 or Info2 and receives Info0 --> no TE connected), there is sometimes corruption on the D channel coming from the TIN pin and going to the DOUT pin.

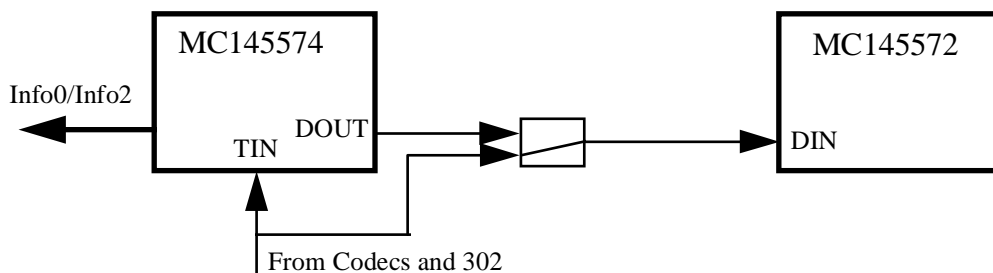
## Workaround for the MC145574:

None

## Workaround for the Smart NT1 application:

A multiplexor (type 74HC157) should be inserted between the Dout pin of the S/T interface and the Din pin of the U interface. this multiplexor should allow to connect Tin pin of the S/T interface directly to the Din pin of the U interface.

### \* No TE connected:



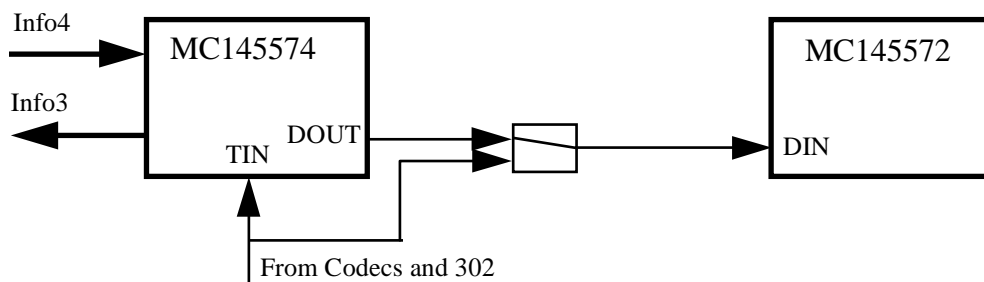
The D data coming from the 302 are sent directly to the U interface.

### \* TE in connection:

The S/T interface activate the TE (Info4/Info3).

- If there is a communication in the D channel just before the TE connection, it should be completed before switching the mux. There is no possibility for a TE to access to the D channel because the S/T interface sends in the E channel the D data coming from the Tin pin.
- If there is a communication in a B channel just before the TE connection, the mux should be switched immediately, some data will be lost but with no audible effect on a voice communication.

**\* TE connected:**



All the 2B+D data coming from the TEs and from the 302+Codecs are processed by the S/T interface and sent to the U interface.

**\* TE in disconnection:**

The S/T interface becomes deactivated, it sends Info0 or Info2 and receives Info0.

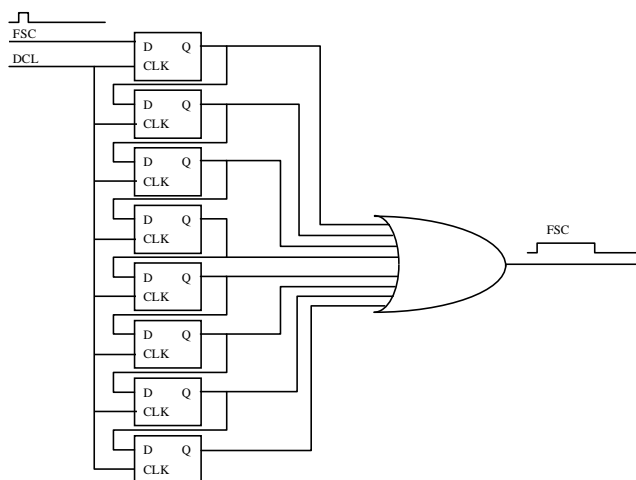
- If there is a communication in the D channel just before the TE disconnection, it should be completed before switching the mux.
- If there is a communication in a B channel (coming from a Codec) just before the TE disconnection, the mux should be switched immediately, some data will be lost but with no audible effect on a voice communication.

## Problem:

In TE Master mode and IDL long frame (8 or 10 bits), there is a corruption of the B1 channel during the transfer of the B1 data from the IDL bus to the S/T loop.

## Workaround:

Program the S/T interface in TE Master mode and IDL short frame (8 or 10 bits). Use some glue logic to transform the FSYNC short frame into a FSYNC long frame. Then, all the other components connected on the IDL bus will work in IDL long frame format.



Circuit to transform IDL short frame into IDL long frame.

## Problem:

In TE Master mode, IDL TimeSlot Assigner mode and DCL = 2.048 MHz or 2.56 MHz, when Drequest and Dgrant are high, there is no transfer of D data from the IDL bus to the S/T loop for some specific D timeslots.

- \* DCL = 2.56 MHz:      timeslots \$00 to \$0B --> no problem  
                                  timeslots \$0B to \$55 --> no transfer  
                                  timeslots \$56 to \$9F --> no problem
- \* DCL = 2.048 MHz:    timeslots \$00 to \$09 --> no problem  
                                  timeslots \$0A to \$44 --> no transfer  
                                  timeslots \$45 to \$7F --> no problem

## Workaround:

- use DCL = 1.536 MHz or 512 kHz.
- or
- program D Channel Procedures Ignored option (BR7(7) = 1).

## Problem:

In TE GCI mode, when the BR7(1) bit, LAPD Polarity Control, is set to 1, the C/I commands which arrive on the DIN pin have an inverted effect on the D channel access request.

If BR7(1)=0:

- AR8 and AR10 request the D channel access
- all the other C/I commands don't request the D channel access

If BR7(1)=1:

- AR8 and AR10 don't request anymore the D channel access
- all the other C/I commands request the D channel access

## Workaround:

- do not use LAPD Polarity Control.
- if LAPD Polarity Control is absolutely required, replace:
  - \* AR8 by AREOM
  - \* AREOM by AR8
  - \* use CLASS pin or NR2(0) to change the class for the D channel operation

**Problem:**

In TE full GCI mode, data on the first B channel is shifted to the right by one bit (i.e. data is corrupted)

**Workaround:**

- Do not program TSA ( Time Slot Assigner ) OR6(6,7) bits. OR6(6,7) are to be used only when in IDL2 mode. Set OR6(6,7) to zero at all times.

**Problem:**

In TE GCI mode, when the BR7(1) bit, LAPD Polarity Control, is set to 1, the C/I commands which arrive on the DIN pin have an inverted effect on the D channel access request.

If BR7(1)=0:

- AR8 and AR10 request the D channel access
- all the other C/I commands don't request the D channel access

If BR7(1)=1:

- AR8 and AR10 don't request anymore the D channel access
- all the other C/I commands request the D channel access

**Workaround:**

- do not use LAPD Polarity Control.
- if LAPD Polarity Control is absolutely required, replace:
  - \* AR8 by AREOM
  - \* AREOM by AR8
  - \* use CLASS pin or NR2(0) to change the class for the D channel operation

**Problem:**

The external S/T loopback is not functional for either TE or NT mode.

**Workaround:**

- The external S/T loopback as defined in Section 9.13 of the *MC145574 Reference Manual* is not functional. If you follow the procedures that are outlined in Section 9.13, data on DIN will not be looped back to DOUT.
- Use the IDL2 loopback mode as defined in Section 8.8 of the *MC145574 Reference Manual*.

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Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku,  
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[support.japan@freescale.com](mailto:support.japan@freescale.com)

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Freescale Semiconductor Hong Kong Ltd.  
Technical Information Center  
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