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MC33742, MC33742S Silicon Mask Errata

INTRODUCTION

This errata applies to MC33742 and MC33742S devices. It describes the specific conditions and events necessary for the occurrence of an unexpected reset. Work around solutions to avoid the reset are also described.

This errata sheet applies to the following product families:

- MC33742DW/R2
- MCZ33742EG/R2 (Pb-Free)

- MC33742SDW/R2
- MCZ33742SEG/R2 (Pb-Free)

DEVICE REVISION/MARKING IDENTIFICATION

The device marking identification is indicated by MC33742DW, MC33742SDW, MCZ33742EG or MCZ33742SEG. All standard devices are marked with a device identification and build information code.

DEVICE BUILD INFORMATION / DATE CODE

Device markings indicate build information containing the week and year of manufacture. The date is coded with the last four characters of the nine character build information code (e.g. “CTKAH0429”). The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the week. For instance, the date code “0429” indicates the 29th week of the year 2004.

DEVICE PART NUMBER PREFIXES

Some device samples are marked with a PC prefix. A PC prefix indicates a prototype device which has undergone basic testing only. After full characterization and qualification, devices will be marked with the MC or SC prefix.

ANALOG L66R, MASK ERRATA - UNEXPECTED RESET

GENERAL DESCRIPTION

Following specific timing between SPI commands and upon a device mode change via an MCR register write command, an unexpected reset could be generated.

The necessary conditions and events required in order to get the unexpected reset are the following:

step 1) Device should be in Stand-by mode or in Normal mode
step 2) SPI_1: write to any register except the MCR register (SPI_1 read is not relevant).
step 3) Delay (value discussed below)
step 4) SPI_2: write to the MCR register to change the device mode (from Stand-by to Normal or Stop, from Normal to Stand-by or Stop)

Depending upon the delay [step 3], the phase of the SCLK signal versus the device internal clock signal will vary. If the phase is matched (internal clock signal edge occurring at same time as external SCLK pulse) a reset will occur approximately 20µs after the MCR write [step 4) SPI_2].

Reset means that the device enters the reset mode, and that the RST pin is set low. Reset mode is entered for a time "T_reset_dur" (ref to device data sheet). After this "T_reset dur" delay, the device will enter the Normal request mode.

The following paragraphs describe in more detail the necessary conditions for the unexpected reset to occur, and the work around to avoid the reset. Two cases exist depending if CS is held low for a single SPI command or for more than one SPI command. They are discussed separately.

In the following figures, only the relevant signals are shown (CS, SCLK and RST). The internal clock and its phase versus external signals is not shown, as it is not visible from the outside.

CASE 1: CS IS TOGGLED AT EACH SPI COMMAND

Occurrence

A reset may occur if the "delay_a1" or "delay_a2" is between 17.6µs and 22.4µs.

Definition of "delay_a1": this is the delay between the falling edge of 7th clock of the SPI_1 and the falling edge of the 8th clock of SPI_2.

Definition of "delay_a2": this is the delay between the rising edge CS of the SPI_1 and the falling edge of the 8th clock of SPI_2.

Note: the 17.6µs and 22.4µs values are derived from the tolerance of the period of the internal clock signal. As stated above, a reset will occur if "delay_a" is within the above window <u>AND</u> if the phase condition are matched. Both conditions are necessary, and this mean that reset will not occur every time "delay_a" is within the 17.6 to 22.4µs window.

Figure 1 below is the illustration for case 1, when both conditions for "delay_a" <u>and</u> "phase" are met.

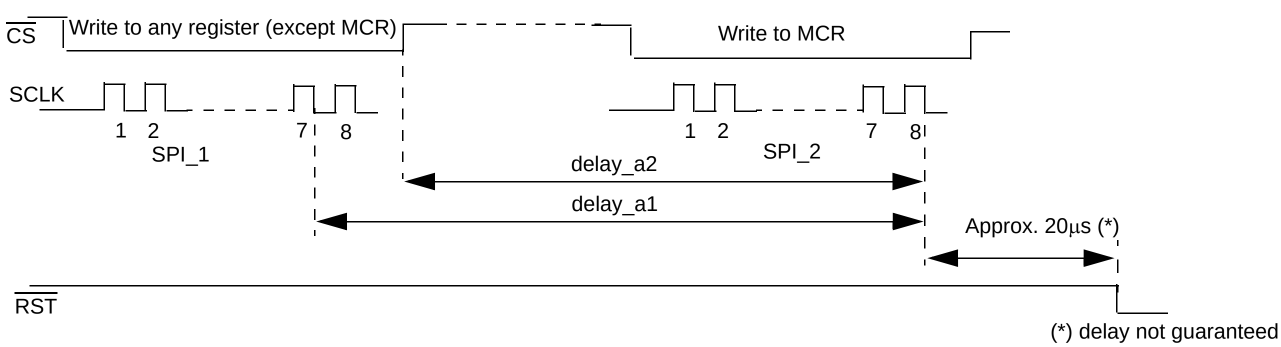


Figure 1. CS low for a single SPI command

WORK AROUND FOR CASE 1:

The work around is to ensure that the "delay_a1" AND "delay_a2" are shorter than 17.6µs or longer than 22.4µs. This will prevent the phase conditions between internal clock signal and SPI signals to be matched.

In order to be safe, the recommendation is to use "delay_a1" longer than 25µs.

Case 2: CS is maintained low for more than one SPI command

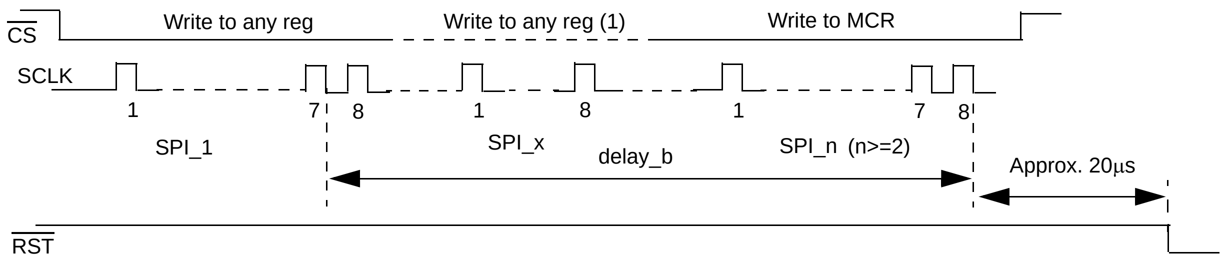
Occurrence

A reset may occur if the "delay_b" between the falling edge of the 7th clock pulse of "SPI_1" and the falling edge of the 8th clock pulse of "SPI_n" is longer than 8.8µs. SPI_n is the last SPI command occurring while CS is held low.

Definition of "delay_b": this is the delay between the falling edge of 7th clock of the SPI_1 and the falling edge of the 8th clock of SPI_n.

Note: the 8.8µs value is derived from the tolerance of the period of the internal clock signal. As stated above, a reset will occur if "delay_b" is greater than 8.8µs <u>AND</u> if the phase conditions are matched. This mean that reset will not occur every time "delay_b" is > 8.8µs.

Figure 2 below is the illustration for case 2, when both conditions for “delay_b” and “phase” are met.



(1): Not same register as previous SPI command, other wise respect “T2spi” delay described in device data sheet

Figure 2. $\overline{CS}$ low for more than one SPI command

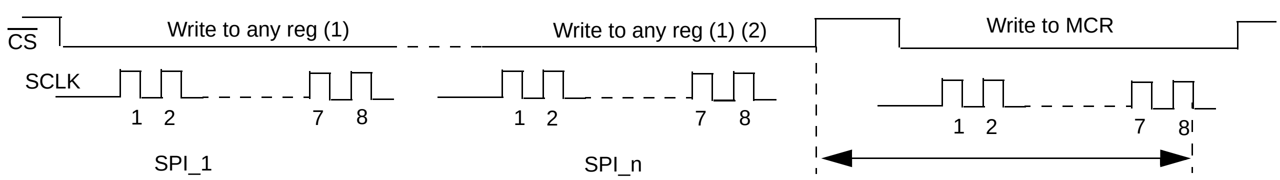
WORK AROUND FOR CASE 2:

If the $\overline{CS}$ has to be maintained low for the series of SPI write commands (which includes the MCR write), “delay_b” must be shorter than 8.8µs. The “delay_b” is considered from the first SPI command occurring after a $\overline{CS}$ low transition to the MCR write command (ref to fig 2), so in the case of many SPI commands (i.e 3 or more) such delay will likely not be met, due to SPI frequency limitation.

A more practical solution is to ensure that the MCR write command occurs with a dedicated high to low transition on $\overline{CS}$, AND to ensure that the delay between the $\overline{CS}$ rising edge of the previous SPI commands and the 8th clock pulse of the MCR write command is greater than 22.4µs.

In order to be safe, the recommendation is to use “T_delay” longer than 25µs.

The work around is illustrated in the figure below:



(1): not MCR
(2): not same register as previous SPI command, other wise respect “T2spi” delay described in device data sheet

Figure 3. work around when $\overline{CS}$ is maintained low for several SPI commands

EXAMPLE OF UNCRITICAL SCENARIOS:

ex1: SPI command “read any register” followed by SPI command “write MCR register” (independent of $\overline{CS}$ operation):

ex 2: Write to MCR register the same content as the previous write to MCR, this mean no device mode change (independent or previous SPI command, write or read, and independent of $\overline{CS}$ operation).

Result: no unexpected reset.

Questions to verify if application is potentially affected.

Below is a list of question which will help to asses if the application is affected by the unexpected reset.

1. What is the impact of an unexpected reset to the application?
2. Is “MCR write” command used?
3. Is the previous SPI a “read” or a “write” command?
4. What is the delay between an “SPI MCR write” and previous the “SPI write”?
5. How is the delay in item 4 compared to “delay_a1” , “delay_a2” and “ delay_b?

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