

MC68302 Errata Revision C.1 (Masks 0F26E, 1F26E)

ERRATA

Errata #1 changed slightly between Revision C.0 and C.1 (both the summary and workaround have changed). None of the following errata are considered serious. At this time Motorola has not released any schedule on when it will be possible to fix these errata.

1. Interrupt Vectors in Slave Mode

Summary:

If the MC68302 is used in slave mode AND and an external asynchronous master is used AND the external master has not performed an internal read cycle since the previous IACK cycle, then during the current IACK cycle, the 302 will drive the previous interrupt vector and the IPR and ISR registers will not be updated.

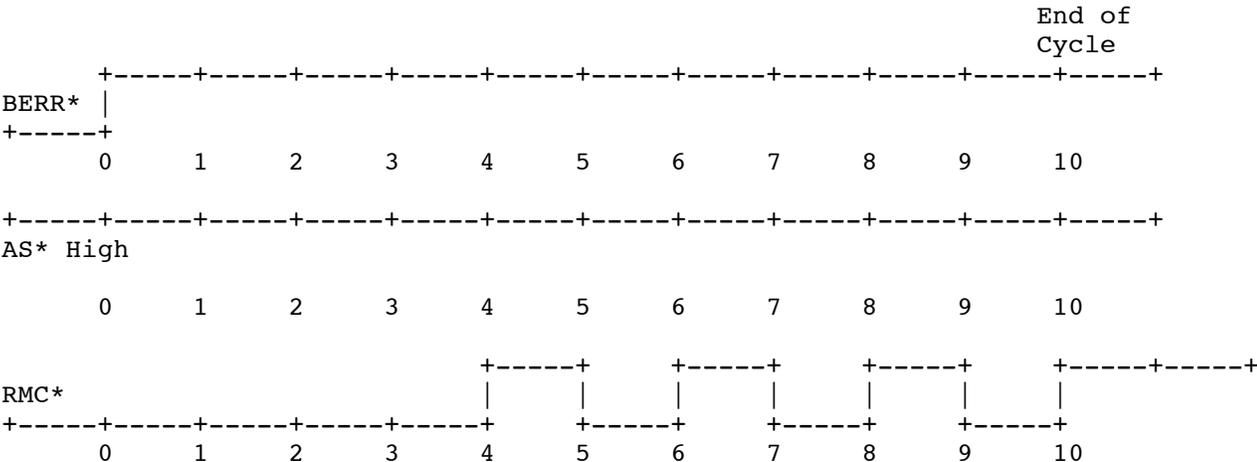
Workaround

- Option 1)** The user should perform an internal read cycle (i.e. read the IPR or ISR or any other internal register) during the Interrupt routine.
- Option 2)** Eliminate One of the Possible Causes - The user may implement a workaround by eliminating one of the conditions listed above, that can cause the bug.

2. RMC* and BERR* During a Read-Modify-Write Cycle (TAS Instruction)

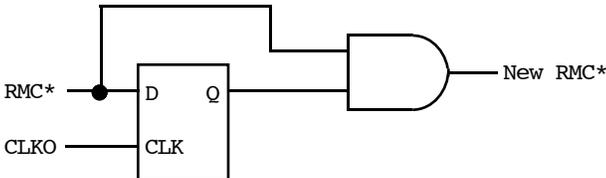
Summary:

When BERR* is either internally or externally generated during a Read-Modify-Write Cycle, the end of the cycle is extended by 10 clocks from BERR* going high, and RMC* oscillates 3 times before being negated at the end of the cycle. The MC68302 waits for RMC* to go High and stay High before it starts handling the bus error. Before the end of the cycle, BERR*, AS*, and RMC* look like the following:



Conclusion:

This problem is not going to be fixed. If a product has to wait on RMC* to go High and stay High, then the following circuit will work and will only cause a 1 clock delay after the 10 clocks of the extended TAS cycle. CLKO is the Clock output of the 68302.



3. Very Short Frames in Synchronous Protocols

Summary:

If a MC68302 SCC is used in a synchronous protocol mode (HDLC, BISYNC, Transparent, or DDCMP), **AND** the transmit frame is stored in just one data buffer, **AND** the transmit frame is only 1 or 2 bytes in total length (i.e. 1 or 2 bytes stored in the data buffer) **AND** more than one MC68302 SCC is operating simultaneously, it is possible after some amount of time (minutes, hours, or days) for a frame to be reported as being transmitted successfully (i.e. the Tx BD shows that it has been transmitted without errors), but in reality, the frame was not transmitted over the TXD pin.

Workarounds:

- Option 1)** In the case of transmitting a two byte frame, simply split the frame into 2 one-byte buffers. This will eliminate the problem, and will not affect serial performance.
- Option 2)** Do nothing. Since the problem occurs very rarely, wait for the missing frame to be detected by the higher layers of the software, and a retransmission requested.

4. BISYNC

Summary:

When external microcode is downloaded into the RAM area of the 68302 (not necessarily operating), **AND** the BISYNC protocol is operating on any channel **AND** { the Hunt Mode bit (H) is set in the BISYNC Control Character Table **OR** a receiver overrun status bit (OV) is set in the Receive Buffer Descriptor **OR** a carrier detect signal status bit (CD) is set in the Receive Buffer Descriptor}, there may be incorrect operation of the BISYNC protocol.

Workarounds:

- Option 1) Eliminate one of the first two essential causes :**
The user may implement a workaround by eliminating one of the first two essential conditions listed above, that can cause the bug.
- Option 2) Eliminate all of the conditions in the third cause :**
 - (i) Do not set the Hunt mode (H) bit in the BISYNC Control Character Table, instead put the channel into Hunt mode by host command (Enter Hunt);
 - (ii) ensure the margins of operation are such that a receiver overrun can never occur; and
 - (iii) permanently connect the SCC's CD* input line to a logic LO to prevent loss of Carrier Detect. The real status of CD may be detected by software using a port connected to the peripheral's CD line.