Device Errata

MC68MH360 QUICC32

Revision E.1. Mask 0F83S

April 4, 1996

These errata items are valid on E.1 silicon. Please note that any errata listed in this document also applies to older revisions, unless otherwise stated. Revision C.1 was the first silicon available of the QUICC32. Revision C.2 mentioned in earlier sheets has been renamed E.1 Revision E.1 is sampling at the time of this writing.

All items changed since the January 26, 1996 Rev E.1 errata sheet are in *Italics*.

CPU32+ Errata

no Errata

SIM60 Errata

1. Parallel I/O pins are not three-stated immediately after Reset

When the QUICC is reset, the parallel I/O pins (Port A, B, and C) are not three stated until the PLL locks. Thus, any port pins that are programmed as outputs may continue driving until the PLL re-locks after reset. This problem will also occur during power-up reset. In this case, the parallel I/O pins will be in an indeterminate state until the PLL locks. The fix for this has not yet been scheduled.

2.Hardware Breakpoint Generation Error

The hardware breakpoint logic will not detect/generate a breakpoint on any address in an 8-bit or 16-bit memory device. The fix has not yet been scheduled.

CPM Errata

1. Spurious SI Sync Pulse Behavior

If:
1) The Time Slot Assigner is programmed to a ram division mode of “00” (One TDM with Static Frames)
AND
2) The Time Slot Assigner is currently processing an entry in the SI RAM past the 32nd entry

AND
3) A pulse is received on the L1SYNC pin (i.e. before the TSA expects a new frame to begin)

The TSA will reset to the first entry in the SI RAM. This will cause the QMC protocol to lose frame synchronization. The workaround is to not use more than 32 entries in the SI RAM. This will be fixed in a future revision.

JTAG Errata

no errata