Chip Errata

MC68VZ328CE/D
Rev.6 12/2003

MC68VZ328 Integrated Processor (DragonBall™ VZ) Chip Errata for Masks: 0K85C, 2K85C, 3K85C, 4K85C, 5K85C and 6K85C

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This document discusses silicon errata information that relates to the 0K85C, 2K85C, 3K85C, 4K85C, 5K85C and 6K85C masks of the MC68VZ328 (DragonBall VZ).

Table 1. Silicon Errata to MC68VZ328

Erratum Number	Erratum Description	Workaround	Applies to Masks
1	EMUCS signal does not function properly (data path not through in CS module).	**Effect:** Cannot start M68VZ328ADS in EMU mode. This signal is used for emulation system development or debug monitor ROM only. User applications normally do not use this function. **Workaround:** The monitor program on the M68VZ328ADS can be programmed in user Flash memory space rather than EMU memory space.	0K85C 2K85C 3K85C 4K85C 5K85C 6K85C
2	EMU enable bit is shorted to Bus break enable.	**Effect:** No usage impact. User can still use hardware break point. **Workaround:** None needed.	0K85C
3	Using SDRAM CAS latency 2, multi-bank configuration, and LCD on simultaneously will cause the system to hang.	**Effect:** The processor cannot be programmed with this simultaneous configuration. **Workaround:** Use CAS latency 1 SDRAM (for 16 MBit) or configure SDRAM to 1 bank rather than 4 banks. This might cause an estimated performance downgrade of less than 2% compared to the original intended configuration.	0K85C 2K85C 3K85C 4K85C 5K85C 6K85C
4	No hysteresis is observed on reset pin and Interrupt I/O pins.	**Effect:** For systems using RC circuit to generate reset signal, placed an external Schmitt trigger buffer (3 pin small IC). **Workaround:** Use external Schmitt trigger device or reset chip.	0K85C

Table 1. Silicon Errata to MC68VZ328 (Continued)

Erratum Number	Erratum Description	Workaround	Applies to Masks
5	Real Time Int Status bits cannot be masked by interrupt enable bits.	**Effect:** Unlike other interrupt status registers, each of these status bits is set when the corresponding event occurs, regardless of its corresponding interrupt enable bit. If a user uses more than one real time interrupt or more than one real time clock interrupt, the following software workaround can be applied. **Workaround:** When an interrupt occurs, service the interrupt only when both its interrupt enable bit and interrupt status bit are set.	0K85C 2K85C 3K85C 4K85C 5K85C 6K85C
6	The clock generation module cannot attain the maximum PLLCLK frequency of 77.7216 MHz.	**Effect:** (Refer to Figure 4-1 of MC68VZ328 User's Manual) The maximum PLLCLK frequency in clock generation module cannot attain 77.7216 MHz. A minimum of 66.32 MHz is guaranteed. This erratum will cause the default bootup system frequency to be lower than 19.4304 MHz in both normal mode and bootstrap mode when a 38.4 kHz crystal is used. The erratum therefore affects the operation of bootstrap mode because the baud clock generated from system clock in UART module will not provide the expected 19200 baud for communication. In short, it is not recommended to run bootstrap mode if the crystal used is not 32.768 kHz. **Workaround:** No workaround is available. Suggest using 32.768 kHz crystal.	0K85C 2K85C 3K85C 4K85C 5K85C 6K85C
7	Cannot read SPI1 RXFIFO during data exchanges.	**Effect:** User cannot read RXFIFO while SPI1 is receiving data bytes. When writes to the RXFIFO, from incoming data, and a user read of the RXFIFO occur simultaneously, the RXFIFO index pointer will not increment and decrement appropriately. User will see a double byte received. **Workaround:** Software workaround exists but throughput will be lowered. When XCH bit deasserts, signalling end of transmission, the user can now read the RXFIFO.	0K85C 2K85C
8	Cannot write to SPI1 TXFIFO during data exchanges.	**Effect:** User cannot write to TXFIFO while SPI1 is transmitting data bytes. When user writes to the TXFIFO and a read to the TXFIFO, from data being transmitted, occur simultaneously, the TXFIFO index pointer will not increment and decrement appropriately. User will see a double byte transmitted. **Workaround:** Software workaround exists but throughput will be lowered. When XCH bit deasserts, signalling end of transmission, the user can now write to the TXFIFO.	0K85C 2K85C

Table 1. Silicon Errata to MC68VZ328 (Continued)

Erratum Number	Erratum Description	Workaround	Applies to Masks
9	SPI1 transmits wrong bit if write to SPI1 TXFIFO during data exchanges.	**Effect:** User cannot write to TXFIFO while SPI1 is transmitting data, i.e. XCH bit remains set. Otherwise, data loaded to data shift register from TXFIFO can be incorrect and thus incorrect data transmitted. **Workaround:** Software workaround is to check XCH bit before writing to TXFIFO. The proper sequence is as follows: 1) Upon TXFIFO empty interrupt, data poll XCH bit for logic low. 2) Write data to TXFIFO, up to 8 data word. 3) Set XCH bit (data exchange starts). **Note:** The injected software overhead of this software workaround is the duration of XCH data polling, which is one data word shifting time. After the last data word is loaded to data shift register, FIFO empty interrupt asserts; however, XCH bit is not clear until the last data bit is shifted out. For high speed data rate, software overhead impact is minimum because XCH bit is cleared quickly after the last data word is loaded to shift register.	0K85C 2K85C 3K85C 4K85C
10	Writes to address locations XXXXXXC0–XXXXXXDF (X = don't care) will also write to address locations FFFFFFC0–FFFFFFDF. Address locations FFFFFFC0–FFFFFFDF are used by IBUFF.	**Background:** The IBUFF is a 32-byte long buffer in bootstrap module and is only used in bootstrap mode for temporarily holding data (machine code) for direct execution by jumping to the starting address of this buffer. FFFFFFC0–FFFFFFDF is the memory map location of IBUFF. **Effect:** 1. The default data (0x4E71 or NOP) in IBUFF can be overwritten by any write to address XXXXXXC0–XXXXXXDF. So, if user puts machine codes to IBUFF and executes, he needs to make sure that a JMP 0xFFFFFF5A is also included at the end of his machine codes in order to let processor return immediately to the bootstrap routine for loading new b-record. In normal case, user doesn't need to include that jump instruction as it has already been placed at the end of IBUFF. 2. The user data in IBUFF can be overwritten by any write to address XXXXXXC0–XXXXXXDF. So, user should execute data in IBUFF before any write to XXXXXXC0–XXXXXXDF. **Workaround:** A revised bbugv program has been made. It is named as BBUGV+ and includes a fix to effect #1.	0K85C 2K85C 3K85C 4K85C 5K85C 6K85C
11	The “Address valid to $\overline{CSx}$ asserted” timing in a chip-select read/write cycle cannot meet specified 20 ns if the previous cycle is a DRAM read/write cycle.	**Effect:** The “Address valid to $\overline{CSx}$ asserted” timing (provided in Tables 19-4, 19-5, and 19-6 of the *MC68VZ328 Integrated Processor User’s Manual*) could be as slow as –5 ns (ECDS = 0) or –5 ns – T/2 (ECDS = 1) in a chip-select read/write cycle after a DRAM read/write cycle. **Workaround:** No workaround is available.	0K85C 2K85C 3K85C 4K85C 5K85C

Table 1. Silicon Errata to MC68VZ328 (Continued)

Erratum Number	Erratum Description	Workaround	Applies to Masks
12	Any change to PC or QC values in PLLFSR for certain VCO frequencies may cause PLL stability issues or jitter.	**Effect/Workaround:** The PLL design allows the VCO operation frequency range of 50 MHz to 80 MHz. For best PLL performance, the recommended range of operation is 60 MHz to 70 MHz. Therefore, setting the nominal/default frequency at 66 MHz already covers the allowable drift introduced by process variation. Any change to PC or QC values in PLLFSR for other VCO frequencies is not recommended.	2K85C 3K85C 4K85C 5K85C 6K85C
13	SDRAM configuration using Continuous Page Mode disabled (CPM=0) and Auto Refresh Mode (RM=0) causes refresh cycle to disappear after LCD access.	**Effect/Workaround:** It is advised to use continuous page mode and program SDRAM to appear as one single bank to the SDRAMC by using the following configuration in SDRAM Control register (0xFFFFFC04): 1. CPM=1 2. BNKADDH=11 and BNKADDL=11	0K85C 2K85C 3K85C 4K85C 5K85C 6K85C

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