Freescale Semiconductor
Errata List

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Rev. 2.1, 06/2008

High Performance Computing Platform II (HPC II) V2 Evaluation Board Errata

1 Overview

This document describes the known errata and limitations of the HPC II reference platform, revision V2. In all cases, if an errata has a work around at the time of board manufacture, it is applied to the system before it is shipped to customers.

Errata are classified into three categories: correctable, uncorrectable, and enhancement requests. The last two categories are not corrected, but may be rolled into possible future revisions of the system (if any).

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2 Correctable Errata

Table 1 lists correctable Taiga errata and their corrections or work arounds.

Table 1. Summary of Correctable Taiga Errata

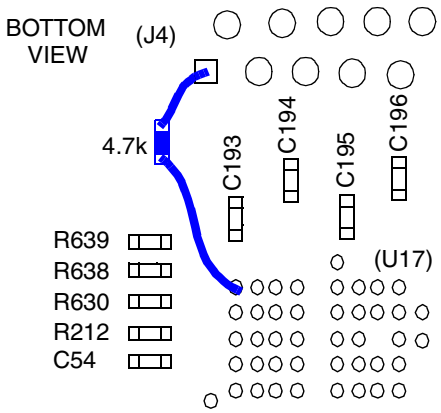
#	Problem/ Respin Resolution	Errata Correction/ Work Around
1	MDIO net requires pull-up resistor. Ethernet PHYs may not function correctly without it. Connect 4.7 kΩ resistor from U17 pin M1 (corner via on bottom of board) to J4 pin 1.	Connect 4.7 kΩ resistor from U17 pin M1 (corner via on bottom of board) to J4 pin 1, as shown below:  Note that on some early boards, a 4.7 kΩ resistor is connected from U11 pin M1 to J22 pin 1. This is also acceptable because the MDIO signal is shared by the PHYs and may be pulled up at either location.
2	U47 VCC not connected to VCC_HOT_5, preventing power switch operation. Correct typo in component property in schematic to “VCC_3.3=VCC_HOT_5.”	Connect U47 pin 5 to U66 pin 5.
3	R10 populated on initial build. None; assembly error.	Remove R10 (top right quadrant of board, between DIMM socket 2 and L2).
4	R114 missing. None; assembly error.	Populate R114 (bottom of board beneath COP HEADER) with 0 Ω resistor.
5	Current limiting prevents TSI108/TSI109 power supplies (VCC_1.2, VCC_1.8, OVDD, and VCC_3.3_REG) from powering up. Either: • Revise current limit estimates and resistor value calculations OR • Change assembly option and component values in schematic.	Reconfigure power limiting as follows: • Remove R325, R330, R332, and R335. • Populate R9, R10, R13, and R14 with 1.5 kΩ resistors. • Change R323, R756, R757, and R773 to 56.2 kΩ resistors. All components are near the respective power supplies.

Table 1. Summary of Correctable Taiga Errata (continued)

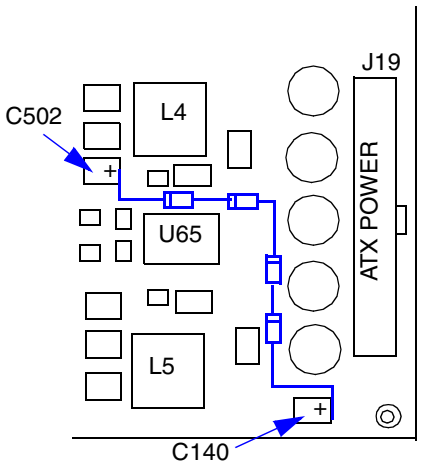
#	Problem/ Respin Resolution	Errata Correction/ Work Around
6	Incorrect FPGA power sequencing: core should ramp before or simultaneous with I/O voltage. FPGA I/O cells drive high until core voltage (VCC_2.5) ramps up. Note that this issue does not appear to cause any improper board operation. Change power sequencing to meet APA150 requirements. (Under review.)	Under review. Preliminary work around of adding 3-diode stack is now superseded by Erratum 9. See also Erratum 7.
7	R127 populated, R132 depopulated on initial build. This further exacerbates FPGA power sequencing issue described in Erratum 6. None; assembly error.	Remove R127, populate R132 with 4.7 kΩ resistor.
8	Only the highest address sector of flash is protected by the FLASH_WP switch (SW3-7). Implement flash write-protection in TICK.	Use software to write-protect flash. Note that the TSI108/TSI109 allows protection of individual banks of the HLP interface via the HLP_B{0..3}_CTRL0 registers. (By default, all banks are write-protected.)
9	U65 PWM #1, which supplies VCC_2.5, not switching when preliminary work around for Erratum 6 (three-diode stack) is implemented. If the diode drops are lower than expected, the VCC_2.5 supply can be above 2.5 V, in which case the switcher does not supply or regulate the voltage. As a result, the VCC_2.5 supply may be powered entirely by VCC_3.3 supply via the diode stack. None. (See Erratum 6.)	As a work around to address Erratum 6, three 1N5817 diodes in series were added between VCC_3.3 (at C140) and VCC_2.5 (at C502). Three diodes has been found to be insufficient, and four are now recommended: 
10	When diode stack is present, which pulls VCC_2.5 rail up with VCC_3.3 (ATX) rail, glitch on VCC_2.5 supply ramp occurs when PWM subsequently begins switching. Under review.	Under review. Preliminary work around of increasing the capacitance of Css (C541) has been found to cause unacceptably slow ramp time of VCC_2.5, resulting in unreliable board operation, and has been retracted.

Table 1. Summary of Correctable Taiga Errata (continued)

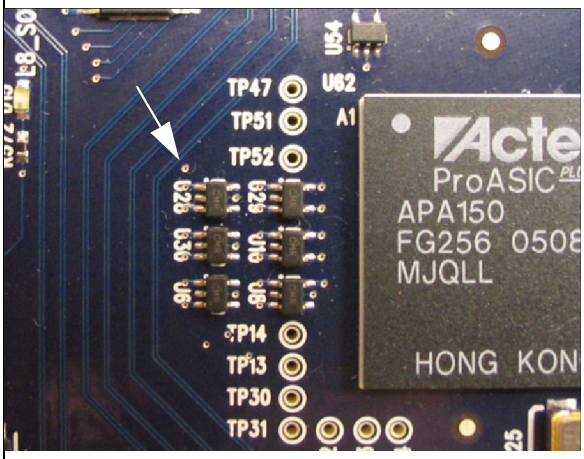
#	Problem/ Respin Resolution	Errata Correction/ Work Around
11	Glitching on PCIRST* signal by FPGA at POR causes erratic SATA behavior. Under review.	Disconnect PCIRST* signal from FPGA by drilling out via near U28, as shown in the figure below. Caution: this via is surrounded by traces on internal layers, in addition to the SATA channel signals on the top layers. Great care must be taken to not damage these traces. A #78 drill bit is recommended. 
12	Due an error in the logic, the following TICK (FPGA) registers are not accessible in Rev 4 of the TICK: • TPWML (inaccessible) • TPWMH (inaccessible) • TISR (inaccessible) • TMON1 (inaccessible) • TDOR (register does not exist) Because the functions of the TDOR register were incorporated into the TMON1 register, TDOR is not implemented in the logic. Note that the TICK revision can be determined by reading the TVER register. (See the *HPC II User's Guide* for more information.) TICK logic fixed in Rev 5 to correct internal register addressing for TPWML, TPWMH, TISR, TMON1. Correct *HPC II User's Guide* to reflect removal of TDOR register.	The inability to access the affected registers prevents the use some advance system features such as CPU fan speed control, but the missing functions are not vital to system operation. If these advanced features are desired, then the TICK must be reprogrammed with the Rev 5 (or later) image.
13	Incorrect buffer causes SATA controller to fail upon board reset. U18 was erroneously replaced with a buffer with bus-hold inputs. The bus hold feature of this buffer interferes with the proper configuration of the SATA controller during board reset, preventing it from properly coming out of reset. Boards on which U18 bears the marking "LXH244A" are affected by this erratum. This includes all boards shipped prior to September 2005 None; BOM change only. Verify that non-bus-hold version of buffer is populated in U18. (Note that part number given in the HPC II schematic is an acceptable part number.)	Any one of the following work arounds allow the SATA controller to be configured correctly during board reset: • Replace U18 with non-bus hold version of buffer. (Example replacement part number: SN74LVC244APW.) • Remove U18. (Note that SATA port presence and activity LEDs will no longer function.) • Replace R240, R241, R207, R246, R247, R248 with 100 Ω resistors.

Table 1. Summary of Correctable Taiga Errata (continued)

#	Problem/ Respin Resolution	Errata Correction/ Work Around
14	R197 and R198 incorrectly labeled as “No_Stuff.” These resistors are incorrectly assigned the No_Stuff property, which indicates they should not be populated during assembly. Remove No_Stuff property from these two components (no changes to design or layout necessary).	Populate R197 and R198 with 0 Ω resistors.
15	Incorrect resistor value for R101. This may cause offset error when attempting to read power consumption of CPU core. Change resistor in schematic and BOM to 0 Ω.	Replace R101 with a 0 Ω resistor.
16	Incorrect voltage level driven to flash reset pins. Flash has 3.3V I/O voltage, but MEM_RST* signal is driven by a 1.8 V buffer, which could potentially result in unreliable flash memory operation. Note, however, that this issue has not been found to have caused errors in any system. Generate a separate FLASH_RST* signal directly from the FPGA output, prior to buffering to create MEM_RST*.	If errors attributed to incorrect flash behavior are encountered, the following steps circumvent the buffer and provide the correct signal level for the reset signals of the flash: 1. Carefully cut traces between vias and pin 12 of U56 and U57 (the vias are located near TP19 and TP20, respectively). 2. Wire pin 12 of U56 and U57 to pin 2 of U54. **Note:** Because this erratum has never been shown to cause system failure, this work around is not applied to systems prior to shipment.
17	TSI109 requires a pull-down resistor on HLP_AD[14] during reset configuration. This configuration option controls the address of the CPU boot code, and boards populated with a TSI109 bridgechip may not boot. The board was designed prior to the release of the TSI109, and this requirement was not known. This requirement does not exist for the TSI108 and this issue does not affect boards populated with that device. Provide pull-up and pull-down options for this signal. **Note:** Not strictly necessary because work around is a legitimate solution to this issue.	Use the modified I^2C EEPROM image for the TSI109. The new image provides the correct reset configuration, performing the same function as a pull-down resistor on HLP_AD[14]. All boards shipped with a TSI109 should already include this image, which will be documented in an upcoming revision of the *High Performance Computing Platform II (HPC II) User Guide* (HPCIIUG).

3 Uncorrectable Errata and Enhancements

The changes listed in Table 2 are either errata which cannot be implemented on the current version of the board, or are requests for enhancements to the board. These changes may be addressed in a revised version of the board, if any should occur. Freescale Semiconductor does not warrant that these issues/requests will ever be addressed.

Table 2. Taiga Uncorrectable Errata/Enhancement Requests

#	Problem/ Respin Resolution	Respin Solution
1	TSI108/TSI109 SD_SYSCLK pin does not have pull-up resistor. Tundra recommends pull-up resistor for this signal. Note that this issue has not been found to have caused failures in any system.	Add pull-up resistor.
2	No decoupling of VCC_1.8 power supply near DIMMs. DIMMs often have few or no decoupling capacitors.	Add bulk and high frequency decoupling capacitors in area around DIMMs.
3	I^2C EEPROM is not write-protectable. Because the EEPROM contains vital configuration settings for the TSI108/TSI109, the board will not boot if the configuration data in the EEPROM is overwritten (see Appendix B in the *High Performance Computing Platform II (HPC II) User Guide* (HPCIIUG)).	Add resistor or switch options to write-protect the EEPROM.

4 Document Revision History

Table 3 provides a revision history for this document.

Table 3. Revision History

Version	Date	Substantive Changes
2.1	06/2008	Clarified Erratum 1 work around description; no significant changes to erratum.
2	03/2007	Added Errata 14, 15, 16, and 17; added Uncorrectable Errata 1, 2, and 3.
1	09/2005	Added Errata 12 and 13; edited Erratum 8.
0	08/2005	Initial release.

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