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MCF5204

Errata to
MCF5204
User Manual

February 10, 2000

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Errata Mask Set: 0H14J and 0K07D

Background Debug Mode

BDM1 - Misaligned WDDATA Operands are Not Captured

When executing the "WDDATA" instruction, certain K-Bus sequences may cause a misaligned operand associated with a WDDATA instruction to not be captured. This restriction applies to word or long-word operands which are misaligned.

Workaround:

Guarantee that all operands referenced by WDDATA instructions are aligned, i.e., 16-bit references on 0-modulo-2 addresses and 32-bit references on 0-modulo-4 addresses.

BDM2- Possible Unexpected Data Breakpoint Trigger

If a data breakpoint monitoring multiple word and byte values is configured, there is a possibility that the breakpoint may falsely trigger. As an example, if the breakpoint hardware is configured to monitor for a certain byte value within a range of addresses, a byte reference is made and the data breakpoint value is present on the data bus, but in a different byte lane, a false trigger could be generated. The logic to fully qualify the reference size and the appropriate bytes of the data bus is incorrect.

Note, this bug does NOT affect the ability to configure a breakpoint of a certain data value at a certain address. The false trigger can only occur when multiple bits in the following fields of the Trigger Definition Register are asserted:

- if multiple bits of TDR[27:26] are set, and a level 2 trigger is enabled, or
- if multiple bits of TDR[25:22] are set, and a level 2 trigger is enabled, or
- if multiple bits of TDR[11:10] are set, and a level 1 trigger is enabled, or
- if multiple bits of TDR[9: 6] are set, and a level 1 trigger is enabled,

then a false trigger may occur

Workaround:

Restrict the use of the data breakpoint to only a single operand, and enable only a single bit in the TDR appropriate for the operand size andlocation on the data bus.

Instruction Cache

I1- Incorrect code fetches can occur if both of the following circumstances apply:

- Cacheable code resides in the uppermost 512 bytes of the 4 GByte address space, i.e., addresses $FFFFFE00 - $FFFFFFFF,
- The external memory access profile allows for 2 wait states or less on the initial transfer of a line fetch, i.e., wait states <= 2-x-y-z, where x,y,z can be any wait state value.

NOTE: The uppermost 512 bytes of address space can be used for KRAM-resident instructions without the possibility of erroneous code fetches. Under any circumstances, there is no possibility for data corruption.

Workarounds include:

- Do not allow execution of cacheable instructions at addresses mapped to the top 512 bytes of the 4 GByte address space. This memory region can be used for KRAM-resident instructions,

or

- If instruction execution at the top of the address space is required, then mark that region as non-cacheable, or mark it as cacheable but require the External memory response to be at least 3-x-y-z.

JTAG OPERATION

During JTAG operation, the act of simultaneously switching numerous outputs to the same logic level may cause the JTAG TAP controller to lose state. The MCF5204 does not exhibit this behaviour during any other operational mode since at no other time can it similarly switch address, data and control outputs simultaneously. For proper JTAG operation, the following conditions must be met:

DC LEVELS

J1 - The following two signals need to be driven outside the published vil/vih levels:

- The compliance enable pins (mtmod) signal input low level (vil) must be driven to 0.6 volts or below.
- The trst/dsclk signal input high level (vih) must be driven to 2.5 volts or above.

INITIALIZATION

J2 - Prior to updating output or bi-directional pins the Boundary Scan Register must be preloaded with lows on odd-numbered pins and highs on even-numbered pins or vice versa. The pins will be defined by the PINOUT diagram on page 13-3 of the MCF5204 USER'S MANUAL (http://www.mot.com/coldfire).

OPERATION

J3 - Once initialization is complete (J2), only the odd pins or even pins may transition as outputs to a different state during an UPDATE-DR instruction.

Timing

T1 - Specs J9/J10/J11/J12 (tTCLTDO, tTCLTDOZ, tTCLBSDV, tTCLBSDZ), tck falling edge to outputs valid, must be relaxed from 30nS to 32nS for all frequencies.

T2 - Spec P4 (tCHPI), clk to Parallel Port Output Hold Time, must be relaxed from 5nS to 3nS for all frequencies.

Bus Operation

B1 - Early external termination of burst cycles not possible

Burst accesses are only executed by the 5204 if the address space (chip select) is configured for internal termination. However, if a burst access is inserting wait states and the user asserts DTACK, the bus cycle should terminate. An internal speed path precludes early termination of burst transfers. Internal termination per the programmed wait states works fine.

Workaround:

Use the internally generated termination for burst cycles.

General Operation

G1 - For improved noise immunity, Motorola recommends placing high frequency, low inductance chip capacitors on the system board as close to the MCF5204 device as possible. A combination of several 0.001uF ceramic, 0.1 uF ceramic and 100 uF tantalum chip capacitors should provide adequate decoupling in the system environment.

Background Debug Mode

SBDM1 - When a BDM command is serially shifted into a ColdFire microprocessor, the debug module requests the use of the KBus to perform the required operation. Under certain conditions, the processor may never grant the KBus to the debug module causing the BDM command to never be performed.

Specifically, the KBus grant may be withheld from the debug module if the processor is executing a tight loop where the entire loop is contained within one aligned longword.

Examples include:

```
        align  4
label1: nop
        bra.b    label1

        align  4
label2: bra.w    label2
```

Workaround:

The workaround is to force the loop to be aligned across two longwords. Given this alignment, the processor will correctly grant the KBUS to the debug module.

MCF5204 Errata Change History:

- Rev 1.1: Initial 0HJ14J 5204 Errata with SBDM1. 7/30/97
- Rev 1.2: Added T1, T2, B1. 9/12/97
- Rev 1.3: Added BDM1, BDM2. 10/1/97
- Rev 1.4: Added I1. 10/14/97
- Rev 1.5: Added D1. 11/11/97
- Rev 1.6: Added J1,J2, J3, G1. 1/13/98
- Rev 1.7: Added mask set 0K07D. 2/10/00

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