



Freescale Semiconductor

32-Bit Embedded Controller Division

MPC5534 Rev 0.1 Errata List

July 31, 2007

Blocks affected

BAM - Boot Assist Module
DSPI - Deserial Serial Peripheral Interface
EBI - External Bus Interface
ECSM - Error Correction Status Module
FLASH - Flash array and Control
FMPLL - Frequency Modulated Phase-Locked Loop
FlexCAN - Controller Area Network Module
JTAGC - Joint Test Action Group Controller
MPC5534 - Overall Device
NPC - Nexus Port Controller
NZ3C3 - e200z3 Nexus Class 3 Interface
Pad Ring - Pad Ring
SIU - System Integration Unit
SRAM - Static RAM
e200z3 - Main Processor Core
eDMA - Enhanced Direct Memory Access
eMIOS - Enhanced Modular Input/Output Subsystem
eQADC - Enhanced Queued Analog to Digital Converter
eTPU - Enhanced Time Processor Unit

Errata and Information Summary

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- Errata 6049 BAM: VLE added to the LENGTH field during serial boot message
- Errata 2237 DMA: Dynamic writes to DMA control register can induce preemption failure
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- Errata 1345 MPC5534: SIU MIDR Revision field is 0x0001, DID[PIN]=0x34
- Errata 1827 MPC5534: CS0/GPIO0 signal not available on 208 BGA
- Errata 3487 MPC5534: Flash settings documentation is incorrect
- Errata 1964 NDEDI: eTPU DID same as the Device DID
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- Errata 2878 eQADC: conversions of muxed digital/analog channels close to the rail
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- Errata 3150 eTPU: STAC bus export may skip 1 count



Errata and Information Details

Errata 2297

Customer Information

TITLE: BAM: Serial download unavailable to last 16 bytes (4 words) of System RAM

DESCRIPTION:

When using the BAM Serial boot download feature, the BAM initializes an additional 4 32-bit words after the end of the downloaded records. This is done to insure that if the core fetches the last instruction of the downloaded code from the internal SRAM while executing the code, it will not prefetch instructions from memory locations that have not been initialized.

Note: if the download image has the exact same size as the internal SRAM, the 20 bytes at the beginning of the SRAM will be written with zero value due to incomplete memory decoding.

WORKAROUND:

When using the Serial download feature of the BAM, make sure that the maximum address of the downloaded code does not exceed the end address of the SRAM minus 16 bytes.

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Errata 6049

Customer Information

TITLE: BAM: VLE added to the LENGTH field during serial boot message

DESCRIPTION:

In serial boot mode, tools download 3 pieces of information: a 64-bit password, followed by a 32-bit start address, and then a 32-bit download length (LENGTH). On devices that support the Variable Length Encoded (VLE) instruction set, the 32-bit LENGTH field has been changed to a 1-bit VLE bit followed by a 31-bit LENGTH. The VLE bit replaces what was the MSB of the LENGTH. Setting the VLE bit to 1 indicates that the downloaded code should be run in VLE mode. Leaving VLE a 0 indicates that the downloaded code should be run in BookE/classic Power Architecture instruction set mode. When the VLE bit is set to 1 the BAM programs EBI, RAM and Flash MMU TLB entries (# 1,2 and 3) with the VLE attribute.



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WORKAROUND:

Set the VLE bit (MSB of the 32-bit LENGTH) in the serial boot download data if the code being downloaded uses (was written in) VLE instructions.

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Errata 2237

Customer Errata

TITLE: DMA: Dynamic writes to DMA control register can induce preemption failure

DESCRIPTION:

If the DMA control register (EDMA_CR) is written while a channel is in the process of being preempted by a higher priority channel, the preemption process may be treated as spurious. In this case, the original channel is not preempted but its priority and preemption enable bit are temporarily replaced with those of the channel that caused the spurious preemption. After the lower priority channel completes its transfer, its original priority is restored and the higher priority channel starts its transfer.

This temporary priority change may cause further blocking of higher priority preempting channels.

WORKAROUND:

Do not use the channel preemption feature or if you use preemption, don't write the DMA control register when a preemptable channel is executing.

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Errata 1123

Customer Errata

TITLE: DSPI: Changing CTARs between frames in continuous PCS mode causes error

DESCRIPTION:

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Erroneous data could be transmitted if multiple Clock and Transfer Attribute Registers (CTAR) are used while using the Continuous Peripheral Chip Select mode (DSPIx_PUSHR[CONT=1]). The conditions that can generate an error are:

- 1) If DSPIx_CTARN[CPHA]=1 and DSPIx_MCR[CONT_SCKE = 0] and DSPIx_CTARN[CPOL, CPHA, PCSSCK or PBR] change between between frames.
- 2) If DSPIx_CTARN[CPHA]=0 or DSPIx_MCR[CONT_SCKE = 1] and any bit field of DSPIx_CTARN changes between frames except DSPIx_CTARN[PBR].

WORKAROUND:

When generating DSPI bit frames in continuous PCS mode, adhere to the aforementioned conditions when changing DSPIx_CTARN bit fields between frames.

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Errata 2264

Customer Errata

TITLE: DSPI: Using DSPI in DSI mode with MTO may cause data corruption

DESCRIPTION:

Using the DSPI in Deserial Serial Interface (DSI) Configuration (DSPIx_MCR[DCONF]=0b01]) with multiple transfer operation (DSPIx_DSICR[MTOE=1]) enabled, may cause corruption of data transmitted out on the DSPI master if the clock Phase is set for leading edge capture DSPIx_CTARN[CPHA]=0. The first bit shifted out of the master DSPI into the slave DSPI module will be corrupted and will convert a '0' to read as a '1'.

WORKAROUND:

There are three possible workarounds for this issue.

- 1) Select CPHA=1 if suitable for external slave devices.
- 2) Set first bit to '1', or ignore first bit. This may not be a workable solution if this bit is required.
- 3) Connect SOUT from the master to SIN of the first slave externally instead of using internal signals. This is achieved by setting the DSPI Input Select Register (SIU_DISR) to set the SINSELx field of the first slave DSPI to '00' and configuring this slave's sin pin and master sout pin as DSPI sin/sout functions respectively. This workaround is suitable only if these two signals are available to be connected externally to each other.

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Errata 4022

Customer Information

TITLE: DSPI: DSPI_B pins split to separate supply, VDDEH10

DESCRIPTION:

The DSPI_B SINB, SOUTB, SCKB, PCS_B[0:2] were separated from the VDDEH6 and are now powered by the new power supply pin VDDEH10. Ball J23 on the 416 package was changed from being a duplicate VDDEH6 pin to being a separate VDDEH10 supply pin. 324 pin package drawings show the VDDE10 ball placement. VDDEH6 and VDDEH10 are combined/shorted internally on 208 packages.

WORKAROUND:

For compatibility to the MPC5554, always power VDDEH6 and VDDEH10 from the same power supply (3.0 to 5.25 volts). If compatibility is not required to the MPC5554, VDDEH10 and VDDEH6 can be supplied by different voltage supplies. This allows one DSPI to operate at a different voltage than the other DSPI modules (3.3 and 5 volts, for example).

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Errata 4031

Customer Information

TITLE: DSPI: DSPI D PCS[3:4] are slow speed pins

DESCRIPTION:

The eMIOS[10:11]/PCSD[3:4]/GPIO[189:190] pins have a pad type of SH (slow speed pad) instead of MH (medium speed pad). While the eMIOS function normally does not require a medium speed pad, when the pin is configured as the Deserial Serial Peripheral Interface D Peripheral Chip Select (DSPI_PCSxD), the slow pad may limit the maximum speed of the DSPI port.

WORKAROUND:

Either don't use the DSPI_D PCS functions on these pins or limit the frequency of the DSPI port to account for the difference in slew rate of the pins. The slow pads have a slew rate of 15 to 200 ns and the medium speed pads have a slew rate of 8 to 100 ns (both with a 50 pF load) depending on the setting of the Slew Rate Control bits in the Pad Configuration register (PCRx[SR]).

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Errata 2379

Customer Information

TITLE: EBI: Calibration pads are 1 ns slower than EBI

DESCRIPTION:

The calibration bus outputs and input setup time is 1ns longer than the equivalent normal External bus signals. Therefore, the electrical specifications need to be added to the data sheets for the calibration signals.

WORKAROUND:

For synchronous (to CLKOUT) peripherals on the calibration pads, make certain that the bus will meet the new electrical specification.

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Errata 2823

Customer Information

TITLE: EBI: Do not access external resources when the EBI is disabled

DESCRIPTION:

When the external bus is disabled in the External Bus Interface Module Control Register (EBI_MCR[MDIS] = 1), accesses through the EBI will not terminate and the master requesting the access will not request another one.

WORKAROUND:

Do not disable the EBI or do not allow accesses to the external bus through Memory Management Unit (MMU) settings in the core. Other internal bus masters (such as DMA) bypasses the MMU and therefore these accesses will hang the external bus if the destination is in the external bus address map.

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Errata 3111

Customer Errata

TITLE: EBI: Dual controller mode cannot be guaranteed under all conditions

DESCRIPTION:

In dual controller mode, the specification for the phase relationship between EXTAL and CLKOUT is +/- 1 ns, however this does not allow adequate set up and hold times to guarantee successful operation of the external bus to a second MCU.

WORKAROUND:

Do not use in Dual Controller mode.

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Errata 3839

Customer Errata

TITLE: EBI: Timed out accesses (external TA only) may generate spurious TS_B pulse

DESCRIPTION:

When an external Transfer Acknowledge (TA) access times out, there is a boundary case where the External Bus Interface (EBI) asserts a Transfer Start (TS) pulse as if starting another access, even if no other internal request is pending. The boundary case is when the access is part of a "small access" set (sequence of external accesses to satisfy 1 internal request), and when the external TA arrives around the same cycle (+/- 1 clkout cycle) as the bus monitor timeout (BMT).

Most EBI signals will stay negated during this erroneous transfer (CS, OE, WE, BDIP). However, along with TS assertion, RD_WR may also assert (for 1 cycle only, during this phantom TS), if the prior access that timed out was a write. This condition can generate an erroneous write transfer (with CS negated). The address (ADDR pins) will be incremented to the address of the next small access transfer that would have been performed, and the value driven by the EBI on the DATA bus (if a write) may change. Busy Busy (BB) may be asserted along with the phantom TS (if external master modes is enabled in the EBI Module configuration Register, SIU_MCR[EXTM]=1), and the Transfer Size (TSIZ) value may change.

Internally, the EBI terminates the timeout access, and the internal state machine goes to IDLE after the timeout access. So the EBI will not be "hung" after the spurious TS, and the EBI does respond properly to future internal or external requests.

However, the side effect of the spurious TS is that it may cause an external non-chip-select device to think an access is being performed to it, resulting in 1 of 2 bad effects (depending on RD_WR value during spurious TS):

- 1) RD_WR high (read): ext. device may drive back read data some number of



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cycles later, possibly conflicting with a future real access (e.g. write) that might have started by that time.

2) RD_WR low (write): ext. device may get an erroneous write performed to it

Note that the soonest possible TS for a real transfer (after the timeout transfer), is 2 cycles after the spurious TS (so 1 cycle gap), meaning this Bug will never result in a 2-cycle TS pulse.

WORKAROUND:

Do not enable bus monitor in the EBI Bus Monitor Control Register (keep SIU_BMCR[BME]=0), unless at least 1 of the following 3 conditions can be met:

1) The external TA will never be asserted from external device within 1 cycle of when the access would be timing out (see NOTE below)

2) No internal requests greater than external bus size will be performed (e.g. doing data-only fetches of 32 bits or less on 32-bit data bus or 16 bits or less on a 16 bit bus only, so a "small access" could never occur).

3) The side effect of this TS pulse driven to non-CS device is judged to be tolerable in system after a timeout error occurs; depends on spec of external device and user requirements for data coherency after a timeout error occurs.

NOTE: Of the 3 above, #1 is easiest to achieve in most systems. If the maximum possible TA latency of the external device is known, the user just needs to set the BMT period more than (external device maximum latency + 2), and this condition will not occur.

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Errata 1651

Customer Errata

TITLE: ECSM: ECC error reported on prefetches outside the flash

DESCRIPTION:

Accessing the last pages of the internal flash array may cause the flash controller to prefetch past the end of the array if the prefetch limits set up in the flash bus interface control register (FLASH_BIUCR) is greater than 1. This will return an ECC error from the array which will be registered in the Error Correction Module (ECSM). In some cases the core will take a data storage exception and in other cases, it will be ignored.

WORKAROUND:



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Since there are only 2 prefetch buffers in the flash, do not use the last 64 bytes of the internal flash.

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Errata 1745

Customer Information

TITLE: FLASH: The ADR register may get loaded with a flash address even through no ECC error has occurred

DESCRIPTION:

The Flash Address Register (FLASH_AR) may be loaded with a flash address when no Error Correction Code (ECC) has occurred. When an ECC does occur, the FLASH_AR is properly set.

WORKAROUND:

Check the Flash Module Control Register ECC Event Error (FLASH_MCR[EER]=1) to check for an ECC error before examining the ADR register. If an error has occurred then the ADR register data is valid. If an error has not occurred then the FLASH_AR data could change on any flash access.

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Errata 1790

Customer Errata

TITLE: FLASH: Stopping the flash during a pre-fetch may freeze the flash

DESCRIPTION:

When running code from the internal flash, the processor may stop executing code if the stop bit in the Flash Module Configuration Register is asserted (FLASH_MCR[STOP]=1) while an instruction pre-fetch is being performed. The normal operation would be for the flash to return an error and cause an exception.

WORKAROUND:

The user should disable flash pre-fetching (FLASH_BIUCR[MOPFE]=0) before disabling the flash via the stop bit (FLASH_MCR[STOP]=0).

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Errata 2371

Customer Errata

TITLE: FLASH: Large blocks limited to 1,000 Program/erase cycles

DESCRIPTION:

The electrical specification for Program/Erase cycling on large Flash blocks (all 128K blocks - Middle Address Space [MAS] blocks M0 and M1, plus High Address Space [HAS] blocks H0 to H3/H7/H11/H19 [depending on total flash size]) has been changed to 1,000 PE cycles minimum. The small blocks (16K, 48K, and 64K - Low Address Space [LAS] blocks L0-L5) are still specified as 100,000 PE cycles minimum.

The data retention specification all blocks is still 20 years for blocks cycled less than 1000 times and 5 years for blocks cycled 1001 to 100,000 cycles (1,000 for large blocks).

WORKAROUND:

Only use the small blocks for EEPROM emulation (LAS L0-L5). Do not use blocks MAS M0/M1 or HAS H0 to H3/H7/H11/H19 (depending on total flash size) for EEPROM emulation requiring greater than 1,000 Program/Erase cycles. Refer to the latest device electrical specifications (Data Sheet) dated July 2007 or later.

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Errata 2419

Customer Information

TITLE: FLASH: Minimum Programming Frequency is 25 MHz

DESCRIPTION:

Programming and erase operations of the internal flash could fail if the clock to the flash (usually the system clock) is less than 25 MHz.

WORKAROUND:

Do not program or erase the flash when the system operating frequency is below 25Mhz.

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Errata 2742

Customer Information

TITLE: FLASH: PRD must be set before setting the flash wait states to 0

DESCRIPTION:

The Pipeline Read Disable (PRD), bit 24 in the Flash Module Control Register (FLASH_MCR, address 0xC3FC_8000), is not documented. PRD should be set at low system frequencies that allow a one clock cycle flash read access.

WORKAROUND:

Set PRD (FLASH_MCR[PRD]=1) before the Read Wait State Control (RWSC) is set to 0 in the Flash Bus Interface Unit Control Register (FLASH_BIUCR, address 0xC3F8_801C).

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Errata 4726

Customer Errata

TITLE: FLASH: Program or Erase operation could fail at -40C if VDD is less than 1.40 volts

DESCRIPTION:

A flash program or erase function may fail, indicated by a cleared Program/Erase Good bit in the Flash Module Configuration Register following a program or erase operation (FLASH_MCR[PEG]=0b0), if the VDD operating voltage is below 1.40 volts (either using an external 1.5 volt regulator or the internal regulator) at -40 degrees Celsius.

WORKAROUND:

Either: 1) Restrict erase and program operation to a minimum VDD greater than 1.40V, [this allows for full specified operating temperature] if using an external 1.5V supply. If the internal regulator controller is used and the proper Freescale recommendations for the VRC circuitry have been met (see data sheet), the internal regulator will hold the voltage above 1.40 volts and will not have a failure;

or

2) Restrict erase and program operation to a minimum ambient temperature of 25C [allows for full specified operating voltage] if using an external regulator that could drop as low as 1.35 volts.

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Errata 715

Customer Errata

TITLE: FMPLL: LOLF can be set on MFD change

DESCRIPTION:

Normally, the Loss of Lock Flag (FMPLL_SYNCR[LOLF]) would not be set if the loss of lock occurred due to changing of the Multiplication Factor Divider bits or PREDIV bits (FMPLL_SYNCR[MFD] or [PREDIV]) or enabling of Frequency Modulation (FMPLL_SYNCR[Depth]>0b00). However, if LOLF has been set previously (due to an unexpected loss of lock condition) and then cleared (by writing a 1), a change of the MFD, PREDIV or DEPTH fields can cause the LOLF to be set again which can trigger an interrupt request if LOLIRQ bit is set.

In addition, changing the RATE bit will also set the LOLF regardless of previous conditions.

WORKAROUND:

The Loss of Lock Interrupt Request enable in the Synthesizer Control Register (FMPLL_SYNCR[LOLIRQ]) should be cleared before any change to the multiplication factor (MFD), PREDIV, modulation depth (DEPTH), or modulation rate (RATE) to avoid unintentional interrupt requests. After the PLL has locked (LOCK=1), LOLF should be cleared (by writing a 1) and LOLIRQ may be set again if required.

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Errata 1037

Customer Errata

TITLE: FlexCAN: writing to an active receive MB may corrupt MB contents

DESCRIPTION:

Deactivating a FlexCAN receive message buffer (MB) may cause corruption of another active receive MB, including the ID field, if the following sequence occurs.

1. A receive MB is locked via reading the Control/Status word, and has a pending frame in the temporary receive serial message buffer (SMB).
2. A second frame is received that matches a second receive MB, and is queued in the second SMB.



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3. The first MB is unlocked during the time between receiving the CRC field and the 6th bit of end of frame (EOF) of the second frame.
4. The second MB is deactivated within 9 CPI clock cycles of the 6th bit of EOF, resulting in corruption of the first MB.

WORKAROUND:

Do not write to the Control/Status word after initializing a receive MB.

If a write (deactivation) is required to the Control/Status field of an active receive MB, either FREEZE the FlexCAN module or insert a delay of at least 27 CAN bit times plus 10 CPI clock cycles between unlocking one MB and deactivating another MB. This will avoid MB corruption, however frames may still be lost.

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Errata 1428

Customer Errata

TITLE: FlexCAN: Transmit Buffers May Freeze / missing frame

DESCRIPTION:

If a received frame is serviced during reception of a second frame identified for that same MB (message buffer) and a new Tx frame is also initiated during this time, the Tx MB can become frozen and will not transmit while the bus is idle. The MB remains frozen until a new frame appears on the bus. If the new frame is a received frame, the frozen MB is released and will arbitrate for external transmission. If the new frame is a transmitted frame from another Tx MB, the frozen MB changes its C/S (control status word) and IFLAG to indicate that transmission has occurred although no frame was actually transmitted.

The frozen MB occurs if lock, unlock and initiate Tx events all occur at specific times during reception of two frames. The timing of the lock event affects the timing window of the unlock event as follows:

Situation A) Rx MB is locked during the 2nd frame. A frozen Tx MB occurs if:

- 1) Both of these events occur in either a-then-b or b-then-a order: a) A new transmission is initiated by writing its C/S between CRC3 (third bit of CRC field) and EOF7 (seventh bit of end of frame) of the 2nd frame.
b) The Rx MB is locked by reading its C/S after EOF6 of first frame and before EOF6 of second frame.
- 2) The Rx MB is unlocked between EOF7 and intermission at end of the second frame.

Notice in this situation that if the lock/unlock combination happens close together, the lock must have been just before EOF6 of the second frame, and therefore the system is very close to having an overrun condition due to the delayed handling of received frames.

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Situation B) Rx MB was locked before EOF6 of the first frame; in other words, before its IFLAG is set. This is a less likely situation but provides a larger window for the unlock event. A frozen Tx MB occurs if:

- 1) The Rx MB is locked by reading its C/S before EOF6 of the first frame.
- 2) Both of these events occur in either a-then-b or b-then-a order: a) A new transmission is initiated by writing its C/S sometime between CRC3 and EOF7 of the second frame.
- b) The Rx MB is unlocked between CRC3 and intermission at end of the second frame.

Notice in this situation that if the unlock occurs after EOF6, the first frame would be lost and the second frame would be moved to the Rx MB due to the delayed handling of received frames.

Situation C) Rx unlocked during bus idle. A frozen/missing Tx occurs if:

- 1) An Rx MB is locked before EOF6 of an incoming frame with matching ID and remains locked at least until intermission. This situation would usually occur only if the received frame was serviced after reception of a second frame.
- 2) An internal arbitration period is triggered by writing a C/S field of an MB.
- 3) The locked Rx MB is unlocked within two internal arbitration periods (defined below) before or after step 2).
- 4) 0xC is written to the C/S of a Tx MB within these same two arbitration periods. This step is optional if a 0xC was written in step 2).

Two internal arbitration periods are calculated as $((2 * \text{number of MBs}) + 16)$ bus clocks where the number of MBs can be reduced by writing to CAN_MCR[MAXMB]. Bus clocks are the high frequency bus clocks regardless of CAN_CR[CLK_SRC] setting.

Additional Notes:

- 1) The received frames can be transmitted from the same node, but they must be received into an Rx MB.
- 2) When the frozen Tx MB's IFLAG becomes set, an interrupt will occur if enabled.
- 3) The timestamp of the missing Tx will be set to the same timestamp value as the last reception before it was frozen.
- 4) If the user software locks the Rx MB before a frame is received, situation A can occur with a single received frame.
- 5) The issue does not occur if there were any additional pending Tx MBs before CRC3.
- 6) If multiple Tx MBs are initiated within the CRC3/EOF7 window (situation A and B) or two internal arbitration windows (situation C), they all become frozen.

WORKAROUND:

If received frames can be handled (lock/unlocked) before EOF6 of the next frame, situations A and C are avoided. If they are handled before CRC3, or lock times are below 23 CAN bit times, situation B is avoided.

If this cannot be guaranteed, situation A) and B) are avoided by inserting a delay of at least 28 CAN bit times between initiating a transmission and unlocking an Rx MB and vice-versa. Typically a system would use a mechanism to selectively add the necessary delay. For example, software might use a global variable to record an external timer value (the FlexCAN timer can't be used as that would unlock) when initiating a new Tx or unlocking an Rx,

and then add the required delay before performing the second action.

Situation C) can be avoided by inserting a delay of at least two internal arbitration periods between writing 0xC and unlocking the locked Rx MB.

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Errata 1831

Customer Errata

TITLE: FlexCAN: receive time stamp may be incorrect

DESCRIPTION:

Unlocking a FlexCAN2 receive message buffer (MB) with pending frame sometime after a second frame is received or transmitted will cause capture of incorrect timestamp if the following conditions are satisfied:

1. A receive MB is locked via reading the Control/Status word, and has a pending frame in the temporary receive serial message buffer (SMB). The MB remains locked while receiving end of frame bit 6 of the pending frame.
2. The locked MB is unlocked anytime after the first bit of ID of another new frame is transmitted on the CAN bus. The new frame may be transmitted from the Flexcan2 or another CAN node.

In these conditions, the timestamp value for the unlocked receive MB will be the timestamp of the new frame and not the timestamp value from reception of the pending frame.

WORKAROUND:

Avoid locking MB during reception of EOF6 i.e. do not lock until corresponding IFLAG bit is set (prevents locking before present frame is received) and guarantee that received frames are handled (lock/unlocked) before EOF6 of the next frame.

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Errata 4414

Customer Information

TITLE: FlexCAN: Corrupt ID may be sent in early-SOF condition

DESCRIPTION:

This erratum is not relevant in a typical CAN network, with oscillator tolerances inside the specified limits, because an early start of frame condition (early-SOF) should not occur.

An early-SOF may only be a problem if the oscillators in the network operate at opposite ends of the tolerance range (maximum 1.58%), which could lead to a cumulated phase error after 10 bit-times larger than phase segment 2.

A corrupt ID will be sent out if a transmit message buffer is identified for transmission during INTERMISSION, and an early-SOF condition is entered due to a dominant bit being sampled during bit 3 of INTERMISSION.

The message sent will be taken from the newly set up transmit buffer (Tx MB), with the exception of the 1st 8 ID bits, which are taken from the previously selected Tx MB.

The CRC is correctly calculated on the resulting bit stream so that receiving nodes will validate the message.

The early-SOF condition is detailed in the Bosch CAN Specification Version 2.0 Part B, Section 3.2.5 INTERFRAME SPACING - INTERMISSION.

WORKAROUND:

- 1) Configure Tx MBs during FREEZE mode, or
- 2) Out of FREEZE mode, configure Tx MBs during bus idle:
 - For networks with low traffic, determine Bus Idle status by reading the Idle bit of the Error and Status register (CANx_ESR[IDLE]).
 - For networks with high traffic, configure Tx MBs after the 3rd bit of intermission, and before the third bit of the CRC field from the next transmission.

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Errata 1834

Customer Errata

TITLE: JTAGC: SAMPLE instruction does not sample input data during board boundary scan testing.

DESCRIPTION:

Executing the SAMPLE instruction should take a snapshot of the input and output signals present at the pins, without interfering with the normal operation of the chip.

For pins configured as inputs, executing the SAMPLE instruction will result in the internally set, off value, of the pad being sampled and not the actual input value of the pin.

WORKAROUND:

Do not expect to sample input pin values when executing the SAMPLE or SAMPLE/PRELOAD instructions when using JTAG. Use the EXTEST and PRELOAD instructions to test connections between devices during boundary scan testing of boards.

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Errata 1345

Customer Information

TITLE: MPC5534: SIU_MIDR Revision field is 0x0001, DID[PIN]=0x34

DESCRIPTION:

The part number field in the MCU Identification Register (SIU_MIDR[PARTNUM]) is 0x5534. The initial Mask revision number (SIU_MIDR[MASKNUM]) is 0x01. The Part Number Identification field in the Nexus Port Controller Device Identification Register/Message (NPC_DID[PIN]) is 0x34.

WORKAROUND:

Software should be aware that the SIU_MIDR[MASKNUM] field can change in the future.

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Errata 1827

Customer Errata

TITLE: MPC5534: CS0/GPIO0 signal not available on 208 BGA

DESCRIPTION:

The CS0/GPIO0 signal is not available in the 208 BGA package. The CS0/GPIO0 signal on ball R1 is not connected internal to the package.

WORKAROUND:

Do not use the CS0/GPIO0 signal in the 208 BGA package.

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Errata 3487

Customer Errata

TITLE: MPC5534: Flash settings documentation is incorrect

DESCRIPTION:

The MPC5534 Reference Manual included incorrect information on settings required for Flash Bus Interface (Flash_BIU). The Address Pipelining Control (APC) and Read Wait State Control (RWSC) should always be set to the same value.

WORKAROUND:

Refer to updated documentation, either the MPC5534 Reference Manual Addendum (dated after August 2006), an updated MPC5534 Reference Manual (if available), the MPC5534 Electrical Specification (Data Sheet dated after August 2006) or refer to the following table for the correct settings for the Address Pipelining Control (APC), Read Wait State Control (RWSC), and Pipelined Reads Disabled (PRD).

Target Frequency (Maximum)	APC	RWSC	PRD
Up to 25 MHz	0b000	0b000	0b1
Up to 50 MHz	0b001	0b001	0b0
Up to 75 MHz	0b010	0b010	0b0
Up to 80 MHz	0b011	0b011	0b0

The Write Wait State Control (WWSC) should be set to 0b01 for all frequencies. For maximum performance, the Data Prefetch Enable (DPFEN) and Instruction Prefetch Enable (IPFEN) should be set to 0b1, the Prefetch Limit (PFLIM) should be set to 0b110, and the bus interface line read buffers should be enabled (BFEN=0b1). In addition, the Master Prefetch Enable (MxPFE) should be set for each of the Master Cross Bar Master ID (not port number). [MxPFE should be set to 0xF for all Master IDs.] APC, RWSC, WWSC, DPFEN, IPFEN, PFLIM, and BFEN are in the Flash Bus Interface Control Register (FLASH_BIU_CR). PRD is in the Flash Module Configuration Register (FLASH_MCR).

Note: this errata was updated 25 August 2006.

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Errata 1964

Customer Errata

TITLE: NDEDI: eTPU DID same as the Device DID

DESCRIPTION:

The Nexus Dual eTPU Development Interface (NDEDI) incorrectly returns the same information as the MPC5534 Nexus Port Controller (NPC) device level information instead of the eTPU part number (0x124) or eTPU version.

WORKAROUND:

Do not rely on the part number or version fields in either the JTAG Identification register or the NDEDI Identification Register (NDEDI_DID) to determine which version of the eTPU is available.

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Errata 1800

Customer Information

TITLE: NPC: MCKO_DIV can be set to 0x0 (1X MCKO)

DESCRIPTION:

The Nexus Port Controller Port Configuration Register MCKO Divider bits (NPC_PCR[MCKO_DIV]) can be set to 0b000 to select a 1X clock rate as the Nexus Auxiliary output port frequency for the MCKO and MDO pins. Note: Depending on the system frequency, this may force the MCKO and MDO pins to switch at a frequency higher than can be supported by the pins. This frequency is 80 MHz, unless specified in the device electrical specification of the Nexus MCKO and MDO pins.

WORKAROUND:

Insure that the maximum operating frequency of the MDO and MCKO pins is not violated if the NPC_PCR[MCKO_DIV] is set to 0b000.

Note: tools may not support 1X mode. Check with your tool vendor.

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Errata 2054

Customer Errata

TITLE: NZ3C3: Nexus I-CNT same for Indirect Branches and Exceptions

DESCRIPTION:



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The e200z3 core Nexus (NZ3C3) transmits a Program Trace Indirect Branch message without indicating if the message was sent due to a taken branch or due to an exception. The instruction count (I-CNT) for an exception now includes branches in the completed I-CNTs.

WORKAROUND:

Trace reconstruction tools should be aware that the I-CNT for Exceptions and for Indirect Branches are now the same. The tool may need to know (from the user or by parsing registers) the exception handler addresses from the Interrupt vector prefix register (IVPR) and the Interrupt vector offset registers (IVORxx). Users also should not jump directly to interrupt handler addresses. Tools can then differentiate between exceptions and indirect branches.

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Errata 2057

Customer Errata

TITLE: NZ3C3: RDY requires TCK to transition

DESCRIPTION:

The Nexus/JTAG Read/Write Access Control/Status Register (RWCS) write (to begin a read access) or the write to the Read/Write Access Data Register (RWD) (to begin a write access) does not actually begin its action until 1 JTAG clock (TCK) after leaving the JTAG Update-DR state. This prevents the access from being performed and therefore will not signal its completion via the READY (RDY) output unless the JTAG controller receives an additional TCK.

WORKAROUND:

When using the RDY signal to indicate the end of a Nexus read/write access, ensure that TCK continues to run for at least 1 TCK after leaving the Update-DR state. This can be just a TCK with TMS low while in the Run-Test/Idle state or by continuing with the next Nexus/JTAG command.

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Errata 2058

Customer Errata

TITLE: NZ3C3: Incorrect data traced on misaligned little endian store



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DESCRIPTION:

The e200z3 core Nexus data trace of a misaligned (across 64-bit boundary) store to a little endian page will transmit the wrong data on the second half of the double word access.

WORKAROUND:

Either:

(1) Do not allow misaligned stores to little endian pages (use a compiler/linker switch if available) or

(2) Do not attempt to run data trace on little endian pages that are accessed with misaligned operations.

(3) Ignore the data on a misaligned 64-bit access that crosses a 64-bit word boundary on little endian memory pages.

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Errata 2408

Customer Errata

TITLE: NZ3C3: RFM not sent for history buffer overflow caused by 'evsel'

DESCRIPTION:

The e200z3 Nexus should send a Resource Full Program Trace message (RFM) message when the predicate instruction history buffer overflows. The RFM message is implemented to avoid lost history information. A RFM is transmitted when the history buffer is full (contains 31 predicate instruction bits plus a stop bit) and either an isel instruction is executed or a conditional direct branch instruction is executed. However, if an evsel instruction is executed, which should also cause the RFM, it will not be transmitted and subsequent messages will contain corrupted history (HIST) information.

WORKAROUND:

Do not use the 'evsel' instruction, or don't use program trace "history mode" when tracing code segments containing an evsel instruction.

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Errata 2538

Customer Information

TITLE: NZ3C3: No sync message generated after 255 direct branch messages in history mode

DESCRIPTION:

When using the branch history mode of direct branch program trace in the e200z3 core, a synchronization message is not transmitted after 255 program trace messages in a row. This will occur if resource full messages are sent and not counted for triggering a sync message indicating that the branch history fields are full. The resource full message is generated when more than 31 direct branches occur without an indirect branch or exception.

WORKAROUND:

Debuggers should account for the possibility that more than 255 messages could be received without a program trace synchronization message by keeping track of the last known program trace address prior to branch history resource full messages.

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Errata 2806

Customer Information

TITLE: NZ3C3: Data Trace of stmw instructions may cause overruns

DESCRIPTION:

If Nexus data trace is enabled on a section of memory that is loaded or stored with a store multiple word (stmw), or load multiple word (lmw for data read traces), an overrun condition could occur, even if the stall on overrun feature is enabled (NZ3C3_DC1[OVC]=0b011). The stmw/lmw instructions can generate up to 16 Nexus trace messages with a single instruction. If there are not 16 queue locations available, an overflow will occur. Stall mode does not stall the core until there are only four locations available in the e200 Nexus message queue. Therefore if a stmw/lmw generates more than four messages, the queue will overflow. The stmw/lmw instructions load or store two 32-bit registers at a time (64-bit stores/loads) if an even number of registers are selected.

WORKAROUND:

If stall mode is enabled (NZ3C3_DC1[OVC]=0b011), limiting store multiple word instruction in a data trace region to store/load 8 registers or less, will improve the chances that an overrun will not occur, but this is dependent on other messages that could be generated simultaneously with the data trace messages. If stall mode is disabled, or stmw instructions with more than 8 registers are stored, accept overruns in the data trace flow.

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Errata 63

Customer Information

TITLE: Pad Ring: Possible poor system clock just after POR negation.

DESCRIPTION:

The pins RSTCFG_B and PLLCFG[0:1] select one of three PLL modes or allows a clock to be injected, bypassing the PLL. When Power On Reset (POR) negates, if the transitions on these pins selects the bypass mode, a poor clock on EXTAL can provide a poor clock to MCU logic no longer reset by POR. The state of that logic can be corrupted.

WORKAROUND:

If the default PLL and Boot configuration (external crystal reference and boot from internal flash) will be used, then negate the RSTCFG pin (=1). For any other configuration, depending on the final mode required, the pins must have the following values on the pins when the internal POR negates.

Final Mode	RSTCFG_B	PLLCFG[0]	PLLCFG[1]
default	1	-	-
external reference	0	1	1
external crystal	-	1	-
dual controller	-	1	-

After POR negates, the RSTCFG_B and PLLCFG[0:1] can be changed to their final value, but should avoid switching through the 0,0,0 state on these pins. See application note AN2613 "MPC5554 Minimum Board Configuration" for one example off the external configuration circuit.

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Errata 64

Customer Information

TITLE: Pad Ring: RSTOUT is 3-stated during the power-on sequence.

DESCRIPTION:

RSTOUT_B is 3-stated during power on reset.

WORKAROUND:

Connect an external pull device to RSTOUT_B during power on reset. This should be pull-down unless an external reset configuration circuit is being used, in which case it should be pull-up. Refer to AN2613 'MPC5554 Minimum Board Configurations' for further information.

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Errata 2059

Customer Errata

TITLE: Pad Ring: ADDR[19:20]/GPIO[15:16] have double pull devices

DESCRIPTION:

Address lines 19 and 20 (ADDR[19:20]) each have 2 internal pull devices.

WORKAROUND:

Expect the pull current to be up to 300 microamps instead of 150 uA when the internal pull devices are enabled on these two pins. By default after reset, the pad configuration registers (SIU_PCR[15:16]) for these pins defaults to pull up device (WPS=0b1) enabled (WPE=0b1).

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Errata 4381

Customer Information

TITLE: Pad Ring: Pin behavior during power sequencing

DESCRIPTION:

The power sequence pin states table in the device data sheet (electrical specification) did not specify the influence of the weak pull devices on the output pins during power up. When VDD is sufficiently low to prevent correct logic propagation, the pins may be pulled high to VDDE/VDDEH by the weak pull devices.

At some point prior to exiting the internal power-on reset state, the pins will go high-impedance until POR is negated.

When the internal POR state is negated, the functional state during reset will apply and weak pull devices (up or down) will be enabled as defined in the device Reference Manual.

WORKAROUND:

The best solution is to minimize the ramp time of the VDD supply to a time period less than the time required to enable external circuitry connected to the device outputs.

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Errata 1532

Customer Errata

TITLE: SRAM: ECC error injection

DESCRIPTION:

The Error Correction Status Module (ECSM) module includes functionality that allows Error Correction Code (ECC) errors to be injected into the SRAM. This allows testing of the ECC circuitry and for testing software routines that handle ECC errors. However, the ECC errors are not injected into the late write buffer (this buffer is used to post all writes). Therefore, if the location with the error being injected also has new data pending in the write buffer, a subsequent read to the location will match out of the write buffer (not from the SRAM) and the injected error won't be a part of the returned data.

WORKAROUND:

After injecting a SRAM ECC errors, clear the late write buffer by (1) running a dummy write cycle or (2) running 2 idle clock cycles.

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Errata 2499

Customer Information

TITLE: e200z3: JTAG Part Identification is 0x0

DESCRIPTION:

The Part Identification Number (PIN) in the e200z3 core JTAG and Nexus device identification messages and register (NZ3C3_DID) is 0x0. The complete e200z3 JTAG ID and DID is 0x07C0001D. This description was updated February 2006.

WORKAROUND:



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Tools that use the e200z3 DID should expect updated values to identify the PowerPC core or use the complete device Nexus Port Controller DID message/register.

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Errata 3415

Customer Errata

TITLE: e200z3: Debug interrupt (IVOR15) can be taken erroneously

DESCRIPTION:

If instruction complete debug events are enabled in the Debug Control Register 0 (DBCR0[ICMP] = 1) and an external interrupt causes a load multiple word, store multiple word, integer divide, or floating point divide instruction to be interrupted prior to completion, a debug interrupt will be taken erroneously instead of the external interrupt. If external debug mode is enabled in the Debug Control Register 0 (DBCR0[EDM] = 1), debug mode will be entered after fetching the first instruction of the debug interrupt handler.

WORKAROUND:

Use the Go+NoExit method of single stepping in the OnCE Command Register (OCMD[GO] = 1, OCMD[EX] = 0) if external debug mode is enabled in the Debug Control Register 0 (DBCR0[EDM] = 1). If single stepping is implemented using instruction complete debug events, disable external interrupts (MSR[EE] = 0) prior to stepping over a load multiple word, store multiple word, integer divide, or floating point divide instruction.

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Errata 5093

Customer Errata

TITLE: eDMA: BWC setting may be ignored between 1st and 2nd transfers and after the last write of each minor loop.

DESCRIPTION:

The eDMA Transfer Control Descriptor Bandwidth Control field setting may be ignored between 1st and 2nd transfers and after the last write of each minor loop. This will occur if the source and destination sizes are equal. This behaviour is a side effect of measures designed to reduce start-up latency. Reference Manuals may fail to mention this behaviour.



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WORKAROUND:

There are 2 possible workarounds:

1) Adjust the Transfer Control Descriptor (TCD) to make the source size not equal to the destination sizes (i.e. ssize = 16 bit, dsize = 32 bit). This delays the write which allows BWC[0:1] arriving from the TCD to be considered in the execution pipeline during start-up.

2) Adjust the TCD so the channel executes a single read/write sequence and then retires. In addition, the channel can be configured to execute a minor loop link to itself which will restart the channel after arbitration and channel start-up latency. The total number of bytes transferred can be controlled by the major loop count.

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Errata 1278

Customer Errata

TITLE: eMIOS: Possible incoherent access in PEA mode

DESCRIPTION:

When reading the eMIOS channel A data register (EMIOS_CADRn) in Pulse/Edge Accumulation mode (PEA), it is possible that the data sampled will not be coherent with the value sampled at the next read of the channel B data register (EMIOS_CBDRn).

WORKAROUND:

If the eMIOS is used in PEA mode, after a read of the A and B data registers, if A is not greater than B, then discard this measurement and read both registers again after a new flag event.

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Errata 1970

Customer Errata

TITLE: eMIOS: Asynchronous reads of the A and B registers in IPM and IPWM modes may not be coherent

DESCRIPTION:



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When using an eMIOS channel in Input period measurement (IPM) mode or input pulse width (IPWM) mode, asynchronous reads of the A and B registers may provide non-coherent values, resulting in either an incorrect period measurement (IPM mode) or an incorrect pulse width measurement (IPWM mode).

WORKAROUND:

The following pseudo code ensures coherent readings by accounting for CPU/eMIOS simultaneous access and checking the FLAG bit.

```
if (channel flag not set)
    return

disable interrupts if enabled

read B(t0)
read A(t0)
read A(t1)
read B(t1)

clear channel flag

if [A(t0) - A(t1)] != 0
    if [B(t0) - B(t1)] != 0
        pulse width = A(t1) - B2(t1)
    else
        pulse width = A(t0) - B(t0)
else
    pulse width = A(t1) - B(t1)

if (counter rollover)
    adjust pulse width

enable interrupts if previously enabled.
```

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Errata 2013

Customer Errata

TITLE: eMIOS: Comparators A and B enabled by writing to A2 and B2 in DAOC mode

DESCRIPTION:

When the eMIOS is in Double Action Output compare (DAOC) mode, comparators A and B are enabled by the transfer of A2 to A1, and B2 to B1. However, writes to A2 and B2 before the transfers occur will also enable the comparators.

The main impact of this issue is that Output Update Disable (OUn) bit in the eMIOS Output Update Disable Register (eMIOS_OUDDR) can not be used to cause both enables to occur at the same time. If the software sets OUn to disable the transfers and afterwards writes to A2/B2, the comparators will



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then be enabled. Then, if the timebase matches A1 or B1 (which have not yet been updated), the match will be recognized. The expected behavior is that the comparators should not be enabled until software clears OUn and the comparators are enabled simultaneously.

WORKAROUND:

When writing to the A2/B2 registers between the time that OUn is set and then cleared, the software should insure that the timebase does not match the old A1/B1 values.

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Errata 2251

Customer Errata

TITLE: eMIOS: Writes to EMIOS_MCR register in IPM and IPWM modes may cause incoherent reads

DESCRIPTION:

When using the eMIOS in Input Period mode (IPM) or Input Pulse Width Mode (IPWM), writing the EMIOS_MCR register between reads of the A and B registers may result in incoherent values.

WORKAROUND:

When using IPM or IPWM modes, the software should not write to the EMIOS_MCR between reads of the A and B registers.

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Errata 2305

Customer Errata

TITLE: eMIOS: OPMWC unable to produce close to 100% duty cycle signal

DESCRIPTION:



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The Center Aligned Output Pulse Width Modulation with Dead-time Mode (OPWMC) of the eMIOS module does not function correctly if the trailing edge dead time is programmed to a value outside of the current cycle time. The OPWMC mode requires that matches occur in the specific order: A, A, and then B, where the first A must match on the up count of the modulus counter, the second A match occurs on the down count of the modulus counter, and the B match occurs on the internal counter. If the programmed B match value is greater than the time required for the modulus counter to count down from the second A match and then up to the first A match of the next cycle, the first A match of the next cycle will be missed and the mode will not function correctly from that point on.

WORKAROUND:

Configure the selected modulus counter time base and the internal counter of the channel in OPWMC mode to count at the same rate. Program the value of the B match (dead time) to a value less than 2 times the programmed A match value.

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Errata 1742

Customer Information

TITLE: eQADC: 50% reference channels reads 20 mv low

DESCRIPTION:

The equation given for the definition of the 50% reference channel (channel 42) of the Enhanced Queued Analog to Digital Converter (eQADC) is not correct. The 50% reference point will actually return approximately 20mV (after calibration) lower than the expected 50% of difference between the High Reference Voltage (VRH) and the Low Reference Voltage (VRL).

WORKAROUND:

Do not use the 50% point to calibrate the ADC. Only use the 25% and 75% points for calibration.

After calibration, software should expect that the 50% Reference will read 20 mV low (2032 +/-4 counts).

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Errata 2247

Customer Errata



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TITLE: eQADC: Leakage on analog input near 5 volts

DESCRIPTION:

The input leakage on analog inputs to the eQADC may not meet the 150 nA specification if the input voltage is near 5 volts.

WORKAROUND:

Keep analog voltages below (VDDA - 200 mV). Alternately, the leakage current will be reduced to normal levels if there is injection current (20 uA minimum) on any VDDEH powered signals (equal or greater than VDDA). (The sum of the injection current on 5 volt digital signals is greater than 20 uA.) This may cause slightly higher leakage currents on the digital pins that are above the VDDEH supply voltage as well.

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Errata 2878

Customer Information

TITLE: eQADC: conversions of muxed digital/analog channels close to the rail

DESCRIPTION:

If the VDDEH9 and the VDDA power supplies are at different voltage levels, the input clamp diodes on the multiplexed digital and analog signals (AN12, AN13, AN14, and AN15) will clamp to the lower of the two supplies.

If VDDEH9 is lower than the VDDA, conversions on these channels will not obtain full scale readings if voltage is close the the VDDA voltage.

WORKAROUND:

When multiplexed digital/analog signals are used as analog inputs, connect VDDEH9 to VDDA and do not use any of the digital functions multiplexed on these pins.

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Errata 3819

Customer Information

TITLE: eQADC : 25% calibration channel sampling requires at least 64 sampling cycles

DESCRIPTION:



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The 25%*(VRH-VRL) calibration channel (ADC channel 44) will not convert to specification with an ADC sample time less than 64 cycles.

WORKAROUND:

For accurate calibration, the 25% calibration channel should be converted using the Long Sample Time (LST) setting for either 64 or 128 ADC sample cycles in the ADC Conversion Command Message (LST = 0b10 or 0b11).

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Errata 1807

Customer Errata

TITLE: eTPU: TCR2, LAST can negate early in High Rate mode

DESCRIPTION:

If the eTPU Angle Counter (EAC) negates the Tooth Program Register (TPR) LAST bit in Normal mode and , without going through Halt, goes into High Rate mode later, the EAC can incorrectly reset the Timer Channel 2 (TCR2) and/or negate LAST at the end of High Rate mode. TCR2 is wrongly reset if LAST was negated when it entered High Rate mode. LAST is wrongly negated if it was asserted during High Rate mode. The TPR{LAST} bit indicates that the last tooth of the tooth wheel has occurred.

WORKAROUND:

Clear the Tooth Program Register LAST bit (TPR{LAST}=0) in the thread that services the transition of the first tooth of the wheel, in other words, the one that negates LAST. This operation is redundant with respect to TPR value, but fixes the EAC state to avoid an error.

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Errata 1846

Customer Errata

TITLE: eTPU: LAST can fail on consecutive teeth

DESCRIPTION:

If the eTPU Angle Counter (EAC) enters High Rate mode with Tooth Program Register Last Tooth Indicator asserted (TPR{LAST}=1), and LAST is written to a one (1) again during High Rate mode, it negates when the EAC goes to Normal mode. This prevents using LAST on two consecutive teeth transition service requests to reset the eTPU Counter Register 2 (TCR2) one physical tooth after the other.

WORKAROUND:

If TCR2 must be reset on consecutive physical tooth detections, assert LAST for the second reset on a match service set for a low TCR2 count, preventing LAST to be asserted in High Rate mode.

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Errata 2477

Customer Errata

TITLE: eTPU: MISSCNT can fail on sequential physical teeth

DESCRIPTION:

If the eTPU Angle Counter (EAC) detects a physical tooth with a non-zero value in the Missing Tooth Counter (MISSCNT) field of the Tooth Program Register (TPR), and during high-rate mode MISSCNT is written a non-zero value, MISSCNT resets at the end of high-rate mode.

WORKAROUND:

If TPR[MISSCNT] is written a non-zero value and must be written a non-zero value after a single physical tooth is detected afterwards, make it happen on a match service on the TCR2 value estimated for the tooth, thus avoiding MISSCNT to be written in high-rate mode.

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Errata 3150

Customer Errata

TITLE: eTPU: STAC bus export may skip 1 count

DESCRIPTION:

If the eTPU Angle Clock (EAC) is enabled and exported on the Shared Time and Counter bus (STAC) then one count may be skipped on random occasions. This only happens when the EAC transitions from Halt or High-rate mode to normal mode and the integer part of the Tick Rate Register (TRR) inside the eTPU is equal to 1. This skip does not occur on the TCR2 bus internal to the eTPU engine generating the angle clock.

WORKAROUND:



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Either (1) use only greater-than-or-equal comparisons on angle counts imported from the STAC bus; or (2) limit the TRR integer part to 2 minimum. If $\text{TRR}(\text{integer}) = 1$ is a needed rate for maximum performance, the new TRR limitation can be compensated by either:

(a) doubling the TCR1 rate (for instance halving the TCR1 prescaler division), or

(b) halving the number of ticks per tooth (sacrificing angle accuracy).

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End of Report

