



TRANSPORTATION SYSTEMS GROUP
CUSTOMER ERRATA AND INFORMATION SHEET
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C3FBIU.CDR3UBUS_02_0
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ERRATA AND INFORMATION SUMMARY

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AR_389 Little Endian modes are not supported

DETAILED ERRATA DESCRIPTIONS

CDR_AR_897	Customer Erratum	MPC565.B
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RCW[15] always comes from the shadow row.

DESCRIPTION:

RCW[15], which enables clearing of the censor bits always comes from the shadow row of the A flash module, regardless of the intended RCW source.

WORKAROUND:

When not using the flash to provide reset configuration, use an erased shadow row in order to allow the censor bits to be cleared. Otherwise, make sure that RCW[15] = 1 in the shadow row.

CDR_AR_918	Customer Erratum	MPC565.B
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VDDA stress failure

DESCRIPTION:

There is a reliability concern on VDDA, the decoupling capacitor can breakdown causing higher than normal current on VDDA. QADC performance is not impaired.

WORKAROUND:

Allow for an additional 60 mA of current on the VDDA supply. Reduce the voltage on the VDDA pin to increase the lifetime.

CDR_AR_917	Customer Erratum	MPC565.B
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PADS: Connect VDDRTC to VDDSRAM1, VDDSRAM2 to VDDSRAM3

DESCRIPTION:

The VDDRTC power supply was shorted internally to VDDSRAM1, VDDSRAM2 has been shorted internally to VDDSRAM3.

WORKAROUND:

Always connect the VDDRTC supply to VDDSRAM1 and VDDSRAM2 to VDDSRAM3.



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CDR_AR_848 Customer Information MPC565.B

PADS: Negative current injection causes QADC conversion errors

DESCRIPTION:

Injection current of more than 1 mA flowing out of the part (negative current) can cause conversion errors on QADC analog input channels at room temperature. During high temperature operation (150 C), this worsens to 0.5 mA flowing out of the part. Negative current injection implies that current is flowing out of the part to the system. To get this condition, a voltage lower than VSS must exist on the channel for current to flow in this manner. Positive injection current is not an issue.

WORKAROUND:

Do not inject current greater than 1 mA out of the part. The QADC64 disruptive input current minimum specification was changed from -3 mA to -1 mA. The maximum disruptive Input current is still +3 mA.

CDR_AR_912 Customer Information MPC565.B

Bit 15 of the Rest Configuration Word is not documented

DESCRIPTION:

Bit 15 of the Reset Configuration Word is not documented in the Reference Manual. Bit 15 is the Interlock Write Select (IWS). This bit determines which interlock write operation should be used during the clear censorship operation. 0 = Interlock write is defined as a write to any UC3F array location. 1 = Interlock write is a write to the UC3FMCR register.

WORKAROUND:

Consult the latest version of the Reference Manual (dated after July 31,2001).

CDR_AR_899 Customer Information MPC565.B

MPC565: Masknum is 0x11

DESCRIPTION:

The Masknum field of the IMMR register was updated from 0x10 to 0x11 to indicate a minor revision of the device mask set.

WORKAROUND:

Update software that reads the IMMR register to read 0x3311 instead of 0x3310 for the PARTNUM:MASKNUM.

CDR_AR_904 Customer Erratum BBC2.CDR3UBUS_04_0

BBC2: Branch targets must be 4 sequential instructions before MTSPR BBC SPR.

DESCRIPTION:

A user application may crash when a BBC SPR is written in a program loop, if the MTSPR is within 4 instructions of a branch target.

WORKAROUND:

1) Make sure that a "mtspr" instruction writing to any BBC SPR register is preceded by four instructions that are not the target of any branch and followed by "isync" instruction, or 2) Disable BTB.



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CDR_AR_905 Customer Erratum BBC2.CDR3UBUS_04_0

BBC2: Disable BTB, or disable data show cycles and restrict store addresses.

DESCRIPTION:

A memory write access on the UBUS with address bits [18:27] that match the following patterns: 0b10 0001 0000 xxxx (0x210X), 0b10 0001 0001 xxxx (0x211X), 0b10 0001 1001 xxxx (0x219X), 0b10 0001 1000 xxxx (0x218X), 0b10 0011 0000 xxxx (0x230X), 0b10 0011 0101 (0x235X), 0b10 0011 1000 (0x238X), 0b10 0101 1000 (0x258X), 0b10 0101 1001 (0x259X), 0b10 0111 1000 (0x278X), or 0b10 0111 1001 (0x279X) or the BBC SPRs representation on the UBUS will wrongly invalidate BTB entries. Note that the "X" - don't care bits and first hex number may be also "6/a/e". This will cause user application performance degradation and crash in some cases.

WORKAROUND:

1) Avoid writing to external memory locations or memory mapped registers at addresses that match the problematic addresses and disable data show cycles on the CALRAM memory range, or 2) Disable the BTB.

CDR_AR_870 Customer Erratum BBC2.CDR3UBUS_04_0

BBC2: Do not use debug mode with BTB enabled, if code has 0x2F30 branch target.

DESCRIPTION:

The BTB (Branch Target Buffer) incorrectly matches in debug mode if there was a change of flow address of 0x2F30 and code from the address resides in the valid BTB buffer when the part enters debug mode. The address 0x2F30 is the debug port instruction register (SPR) address that the core issues to the BBC in debug mode for instruction fetches. The debug tool may lose communication with the part since the debug port will not assert the "ready" status (DSDO pin "low") until reset.

WORKAROUND:

Do not use debug mode on applications running with the BTB enabled if there is a branch with a target address of 0x2F30. Alternately, either do not enable the BTB in debug mode or do not put any code at 0x2F30.

CDR_AR_793 Customer Information BBC2.CDR3UBUS_04_0

BBC2 Compression: No Compressed Code in Addresses \$FFF00000 to \$FFFFFFF

DESCRIPTION:

IMPU translates addresses in compression mode regardless of address form. Note that this bug may have a minor application impact. It will cause a failure ONLY if the compressed address space covers \$FFF00000 to \$FFFFFFF and the BBCMCR[ETRE] and BBCMCR[EIR] are set, enabling Exception Table Relocation and Enhanced External Interrupt Relocation.

WORKAROUND:

Do not put compressed code at addresses \$FFF00000 to \$FFFFFFF if Exception Table Relocation or Enhanced External Interrupt Relocation are enabled by BBCMCR[ETRE] and BBCMCR[EIR].



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CDR_AR_838 Customer Information BBC2.CDR3UBUS_04_0

Do not set BCMEE bit in the BBCMCR

DESCRIPTION:

No performance improvement is expected for the branch instructions BC and BL when setting BCMEE bit in BBCMCR.

WORKAROUND:

BCMEE should be written to 0 in the BBCMCR.

CDR_AR_914 Customer Erratum C3FBIU.CDR3UBUS_02_0

UC3F: Set censor operation requires a Reset to read Censor bits

DESCRIPTION:

During the internal verify read of a Censor Set operation, the internally unselected censor wordline are not driven to the appropriate voltage. Subsequently, the verify read may update the Censor registers with invalid data and may inadvertently place the UC3F into Information Censorship mode. Only registers bits that should be read as zero may incorrectly be read as a one. Accesses to the array may also produce invalid data.

WORKAROUND:

The UC3F module requires a Reset Operation after any Program or Erase Operation to the Censor[0:1] bits in the UC3FMCR register.

CDR_AR_815 Customer Information C3FBIU.CDR3UBUS_02_0

UC3F: Set small and remainder blocks to same access attributes

DESCRIPTION:

Small blocks require the same attributes (supv/user and data/data&instr) as their remainder blocks. Failure to set this configuration may result in bus error on access to a remainder block.

WORKAROUND:

If the SBSUPV bit for a small block is set as supervisor, then the SUPV bit for the remainder of the block must also be set as supervisor. If the SBDATA bit for a small block is set as data only, then the DATA bit for the remainder of the block must also be set as data only.



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CDR_AR_755 Customer Information DLCMD2.CDR3IMB3_04_0

DLCMD2 switching into 1x-4x mode

DESCRIPTION:

If 4x mode is entered before the symbol counter value reaches the normal mode TIFS value but after the counter has passed the 4x mode TIFS value, the module will hang. Before a transmitter can send an SOF (which resets the symbol counter) it must wait for either of the two following conditions. One, TIFS must have been reached. Two, REOF and a rising edge from another module must have been detected. The second condition means that if another module tries to access the bus before TIFS and after REOF then we can also contend and try and gain access to the bus. If no other module is trying to access the bus then condition two won't occur. The symbol counter does not reset when the mode is changed. This means that if the module is put into 4x mode before the normal mode TIFS value has been detected (which would signal an SOF and reset the counter) the module will keep counting until it reaches its max value and holds. Since the counter is stuck at its max value the module can never detect any symbols on the bus so it will hang until reset.

WORKAROUND:

TIFS must be waited for before changing to 4x mode. To wait for TIFS the difference between the normal mode REOF and TIFS values must be found manually based on their values in the SDATA register. Once that value is determined, wait for bus_idle (REOF), which can be polled for, plus (TIFS - REOF) amount of time. Assuming all cycle counts for normal mode parameters are greater than or equal to the cycle counts for the 4x parameters, no delay (waiting for TIFS) is needed to transition from 4x to normal mode. Note that the bus should be idle when the transition takes place (regardless as to whether the DLCMD2 has detected idle or not) as it is always a bad idea to transition between modes during a message.

CDR_AR_772 Customer Information DLCMD2.CDR3IMB3_04_0

DLCMD2 Equating Parameter Values

DESCRIPTION:

If certain symbols are assigned the same counter value, one of the symbols might never be recognized. Instead the other symbol with the same value would be detected. For example, if RMIN=TSHA than an active RMIN will never be recognized. In the hardware implementation the parameter values are checked with a priority scheme. Once a parameter matches, no further checking is done until the next clock cycle when the counter value has changed. For an active pulse the following parameters are checked in order: TSOFF, TSHA, TLNA, TBRK, RMIN, RSH, RLN, and REOF. In order for each parameter to be detectable they must all have unique values. Similarly, during a passive pulse the following parameters are checked in order: TSHP, TLNP, TIFR, TIFS, RMIN, RSH, RLN, REOF. Again, this set of passive parameters must be distinct. Keeping these parameters distinct is almost guaranteed due to the timing requirements of the J1850 specifications. Certain round trip delays in the transceiver may suggest that some parameters should be equated. In this case either parameter should be adjusted to make them unique. The real risk of equation parameters occurs in test mode when parameters are set as small as possible to accelerate testing.

WORKAROUND:

Parameters in the active set must all be distinct and parameters in the passive set must all be distinct.



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CDR_AR_785 Customer Information DLCMD2.CDR3IMB3_04_0

DLCMD2 RFIFO Polling

DESCRIPTION:

Reads from the staus/rdata word result in valid data being popped from the RFIFO. If the FIFO is empty no pop occurs. This behavior is implemented as follows. First, the status and data at the head of the FIFO is returned. If the FIFO is currently empty, the status register will indicate this and the FIFO data returned will be invalid. After the read has completed, the FIFO will be popped if not empty. The problem occurs if data has been pushed since the status register read indicated an empty FIFO. In this case, when the pop is requested, the FIFO contains valid data which is then popped and lost.

WORKAROUND:

When polling for data, access the status register with a byte read access. Upon finding valid data present in the FIFO, access both the status and data with a word read access.

CDR_AR_771 Customer Information DLCMD2.CDR3IMB3_04_0

DLCMD2 SEL bit is not lockable.

DESCRIPTION:

The spec states that if LCK=1 writes to the SEL bit are disabled. This is not the case. The SEL bit can still be written when LCK=1. This allows the user to read both the 1x SDATA parameters and the 4x SDATA parameters. If writes to the SEL bit were not allowed, after the LCK bit was set it would only be possible to view one set of SDATA parameters depending on the state of the SEL bit when the LCK bit was set.

WORKAROUND:

This is the desired operation of the DLCMD2. The reference manual will be updated to reflect this operation.

CDR_AR_929 Customer Erratum MIOS14.CDR3IMB3_02_0

MIOS: Problem with DASM Duty Cycle Change to 0%

DESCRIPTION:

If the MIOS DASM is used for a OPWM function, a problem occurs if the duty cycle is changed to 0%. The module finishes the current cycle and then it generates one period with 100% duty cycle before it switches to 0% duty cycle.

WORKAROUND:

The workaround is to change the MIOS DASM DataA register to match the DataB register instead of changing the DataB register to match the DataA register.



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CDR_AR_841 Customer Information MIOS14.CDR3IMB3_02_0

MIOS14: Match value intermittently ignored in OC mode when writing a new value

DESCRIPTION:

On B register update of an OC channel (B is NOT double-buffered) the update should enable the compare and match of the B register to the relevant Time Base. If the B register update is done in a time when a match (Not enabled) to the previous B value occurs, the compare and match mechanism will NOT be enabled for the new value.

WORKAROUND:

When updating the B register in OC mode write it twice.

CDR_AR_922 Customer Information PADRING.565_CDR3_02_1

PADS: VOH2.6 Spec changed to 1 mA

DESCRIPTION:

The IOH specification for all 2.6 volt outputs has been changed from 2 mA to 1 mA to insure a VOH2.6 of 2.3 volts. An additional specification has been added for VOH2.6A for a 2.0 mA load with a minimum VOH of 2.1 volts.

WORKAROUND:

2.6 volt outputs will only drive 1.0 mA with a VOH of 2.3 volts and will drive 2.0 mA with an output voltage of 2.1 volts minimum.

CDR_AR_907 Customer Information RCPU.CDR3LBUSIBUS_16_1

RCPU: Issue ISYNC command when entering debug mode

DESCRIPTION:

If the ICTRL[28] bit is set (non-serialized mode) then the RCPU issues two instruction fetch requests into the instruction pipeline after entering debug mode. The debug port and the debug tool may get confused when processing an "mtspr DPDR,Rx" instruction. The debug tool loses synchronization with debug port and receives the wrong data for the "Rx" register. The typical case is when the debug tool tries to save scratch registers or read the debug mode cause.

WORKAROUND:

Issue an ISYNC instruction to the debug port prior to any other instructions when the RCPU enters debug mode after running code.

CDR_AR_440 Customer Information RCPU.CDR3LBUSIBUS_16_1

RCPU: Execute any IMUL/DIV instruction prior to entering low power modes.

DESCRIPTION:

There is a possibility of higher than desired currents during low power modes. This is caused by a possible contention in the IMUL/DIV control area. This contention may only exist prior to the execution of any IMUL/DIV instruction.

WORKAROUND:

Execute a MULLW instruction prior to entering into any low power mode (anytime after reset, and prior to entering the low power mode).



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CDR_AR_214 Customer Information RCPU.CDR3LBUSIBUS_16_1

Only negate interrupts while the EE bit (MSR) disables interrupts

DESCRIPTION:

An IRQ to the core, which is negated before the core services it, may cause the core to stop fetching until reset.

WORKAROUND:

Interrupt request to the core should only be negated while interrupts are disabled by the EE bit in the MSR. Software should disable interrupts in the CPU core prior to masking or disabling any interrupt which might be currently pending at the CPU core. For external interrupts, it is recommended to use the edge triggered interrupt scheme. After disabling an interrupt, sufficient time should be allowed for the negated signal to propagate to the CPU core, prior to re-enabling interrupts. For an interrupt generated from an IMB module, 6 clocks is sufficient (for IMBCLK in 1:1 mode).

CDR_AR_915 Customer Erratum QADC64E.CDR3IMB3_03_0

QADC64E: Conversion Clock cannot be shared between Master/Slave Modules

DESCRIPTION:

In a multiple QADC64E module configuration it is not possible to operate the modules on synchronous conversion clocks. The conversion clock of a module configured as Master cannot be input to the Slave module using the ext_aqadcclk signal.

WORKAROUND:

If simultaneous conversions are required, the customer can trigger both QADC64E modules SIMULTANEOUSLY using the external trigger inputs (ETRIG1 or 2), however, the conversions will not be performed SYNCHRONOUSLY. There is no workaround to allow synchronous QADC64E module operation.

CDR_AR_846 Customer Information READI.CDR3LBUSUBUS_02_0

READI: Synchronize the MCKI input clock to the MCKO output clock.

DESCRIPTION:

The READI module may not properly receive input messages if the input clock is not synchronous with the output clock.

WORKAROUND:

Synchronize the MCKI input clock to the MCKO output clock.



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CDR_AR_924 Customer Information READI.CDR3LBUSUBUS_02_0

READI: Communication is lost when clock freq. is changed while in BDM mode.

DESCRIPTION:

When the READI is being used for BDM, a deadlock occurs when the development tool tries to enter a low-power mode or change the clock frequency (via the debug port). The internal clock will still run at the previous frequency. If code running on the target is changing the frequency then the following will occur: All READI MDI/MSEI traffic is ignored when this change is recognized; All MDO messages in the transmit FIFO will be sent; Then the MCKO will be stopped until the PLL has relocked at the new frequency.

WORKAROUND:

Do not change the system clock frequency from the Nexus debug port. Use code running on the target to change the clock speed. Reset the READI module by asserting sreset_b or hreset_b to continue debugging after unsuccessfully changing the clock frequency.

CDR_AR_698 Customer Information READI.CDR3LBUSUBUS_02_0

READI Input message requires 2 MCKI idle after READI Enabled.

DESCRIPTION:

If an input message is sent to the READI immediately after deassertion of RSTI_B (enabling READI) the READI may not recognize the start of the message and will ignore it. This behavior could cause the tool to get out of sync with the READI.

WORKAROUND:

Do not send in an input message until at least 2 MCKI after READI is enabled, or better, until the DID message is received from the READI.

CDR_AR_783 Customer Information READI.CDR3LBUSUBUS_02_0

READI input messages must be 4 MCKI apart.

DESCRIPTION:

READI input messages must be spaced by at least 4 MCKI input clocks.

WORKAROUND:

Wait for an output message response before sending in another input message.



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CDR_AR_627 Customer Information TPU3.CDR3IMB3_03_0

TPU: (Microcode) Add neg_mrl with write_mer and end_of_phase

DESCRIPTION:

Wrong generation of 50% duty cycle is caused by the command combination "write_mer, end". If the write_mer is the last instruction together with the end, this may create an additional match using the old contents of the match register (which are in the past now and therefore handled as an immediate match)

WORKAROUND:

Add neg_mrl together with the last write_mer and with end-of-phase. The negation of the flag overrides the false match which is enabled by write_mer and postpones the match effect by only micro-instruction. In the following micro-instruction the NEW MER value is already compared to the selected TCR and no false match is generated. The neg_mrl command has priority over the match event recognition, separating the write_mer and the end command. This gives enough time for the new MER to update before the channel transition re-enables match events.

CDR_AR_925 Customer Erratum USIU.CDR3UBUS_10_1

USIU: TEXP feature does not function when VDD supply is low

DESCRIPTION:

The TEXP function does not work if the main power supplies are powered down. Whenever VDD (low voltage supplies other than KAPWR and VDDSRAM) is powered down, hreset_b will be asserted by the chip and low power mode exited. The TEXP pin will never be asserted.

WORKAROUND:

The TEXP pin will never be asserted if VDD is powered down. Use an external counter to indicate the length of power down. As an alternate solution, put the part into Deep Sleep mode to reduce power consumption and leave the power supplies powered.

CDR_AR_909 Customer Erratum USIU.CDR3UBUS_10_1

USIU: Do not assert cr_b to abort pending store reservation access

DESCRIPTION:

If an external cancel reservation (cr_b) is asserted then a pending store reservation may show on the external bus. This may occur with or without transfer start (ts_b), and will terminate after 1 clock. If the region is in the memory controller of the chip generating the store with reservation, then no chip-select or other memory controller attributes will assert on the bus, and the memory will not be altered.

WORKAROUND:

1) Do not assert cr_b; or 2) following assertion of cr_b, external logic must prevent the erroneous store with reservation bus cycle from altering memory, and must not assert ta_b to terminate the erroneous store with reservation bus cycle.



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CDR_AR_910 Customer Erratum USIU.CDR3UBUS_10_1

USIU: RTC may not work when SCCR[RTDIV] is 0

DESCRIPTION:

When the RCPU RTC is set to run with a predivider of 4 using the SCCR[RTDIV] then the RTC may not count at all operating conditions

WORKAROUND:

Set SCCR[RTDIV] to a value of 1 (reset value)

CDR_AR_868 Customer Erratum USIU.CDR3UBUS_10_1

USIU: Do not rely on censorship to prevent access on parts with internal Flash

DESCRIPTION:

Under certain conditions, the flash censorship mechanism can be over-ridden (i.e. loads from flash will return the correct data). This does not apply to parts that do not have internal flash memory.

WORKAROUND:

Do not depend on censorship mechanism to prevent access to the internal flash.

CDR_AR_865 Customer Information USIU.CDR3UBUS_10_1

USIU: Do not rely on the VDDSRAM Low Voltage Detect Circuit

DESCRIPTION:

At temperatures above room ambient (25C), the VDDSRAM low voltage detect circuit may not always indicate that the VDDSRAM voltage has dropped below the minimum data retention level for the SRAM.

WORKAROUND:

Utilize an external mechanism for detecting when the voltage supplied to the VDDSRAM pin(s) is below the minimum data retention voltage.

CDR_AR_833 Customer Information USIU.CDR3UBUS_10_1

USIU: Do not TEA data showcycles or enable data show cycles in single chip mode

DESCRIPTION:

The chip may stop fetching instructions until Reset is asserted if TEA is asserted in data show cycles. This can also occur if the chip is in single chip mode (no databus) since the chip will assert TEA.

WORKAROUND:

Do not assert TEA on data showcycle accesses. Do not program data show cycles when in single chip mode (i.e. no databus is available).



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CDR_AR_869 Customer Information USIU.CDR3UBUS_10_1

USIU: Do not enable ORx[SST] with SCCR[EBDF]>0

DESCRIPTION:

When EBDF>0 an external burst access with short setup timing will corrupt any USIU register load/store

WORKAROUND:

Do not enable ORx[SST] while EBDF>0

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Little Endian modes are not supported

DESCRIPTION:

The little Endian modes are not functional.

WORKAROUND:

Do not activate little endian modes. The reference manual will be updated to remove all little endian mode references.