Silicon Errata for the MSC8101 Processor, Mask 1K42A

This document presents the errata for the 1K42A mask of the Freescale MSC8101 device. The errata are classified and numbered, and each erratum is provided with a description and workarounds. **Table 1** lists the mask numbers and the corresponding versions of the MSC8101 device.

Table 1. MSC8101 Mask Numbers and Revisions

MASK NUMBER	REVISION
0K40A	Rev0
1K42A	Rev0.1
2K42A	Rev0.2
1K87M	RevA
2K87M	RevA.2

Table 2. Silicon Errata

Errata Number	Errata Description	Applies to Mask
SIU1	**Wrong Timer Advancement on RCCR** **Date Added:** 5/30/2000: **Description:** MSC8101 and MPC826X treat the RCCR[TIMEP] value (UC timer) differently then QUICC. In QUICC the timer advanced (N+1)*1024 cycles and in MSC8101/MPC826X the timer advances N*1024 cycles. **Workaround:** None **System Number:** 1399 **Fix Plan:** Rev A	1K42A

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
SIU4	**Incorrect Masking of MCP** **Date Added:** 5/30/2000: **Description:** MCP (Machine Check Interrupt) due to data errors (parity / ECC) is masked by the SWRI bit in SYPCR. **Workaround:** Clear the SWRI bit in SYPCR to get data errors indication. **System Number:** 3695 **Fix Plan:** Rev A	1K42A
SIU8	**Parity Checking Error** **Date Added:** 6/13/2000: **Description:** During a read from a device with port size less than 64 bits, from an address not aligned to 64 bits, the parity bits for parity check are not taken from the correct locations. For example, for a read of 4 bytes from a 32-bit port size from address 4, the parity is checked against DP[4–7] while it should be checked against DP[0–3]. The bug exists for both normal and rmw parity, and for both PowerPC and Local buses. **Workaround:** None **System Number:** 5839 **Fix Plan:** RevA	1K42A
SIU9	**Bus Monitor Asserts Spurious $\overline{\text{TEA}}$ After Address Retry.** **Date Added:** 1/28/2001 **Description:** The bus monitor will not recognize the competition of an Address Retry transaction and will assert TEA if there is no bus activity for a time equal to the expiration time. **Workaround:** Disable the bus monitor in systems where Address Retry cycles are used (e.g. systems which include PowerSpan). **Fix Plan:** Rev A	1K42A
SIU10	**Strict Enforcement of Requirement to Assert $\overline{\text{DBG}}$ and $\overline{\text{TS}}$ in Same Cycle When Core Enabled** **Date Added:** 1/28/2001 **Description:** This is a compatibility note. An external arbiter must assert $\overline{\text{DBG}}$ in the same clock in which $\overline{\text{TS}}$ is asserted (there may be a one clock delay if the PPC_ACR[DBGD] bit is set, however, after reset this bit is not set by default). Some external arbiters, including the one implemented in PowerSpan, violate this requirement. As a result, the system hangs following the first bus access after reset. **Workaround:** Use only a compliant external arbiter or the internal MSC8101 arbiter. **Fix Plan:** Rev A	1K42A
SIU13	**SDAMUX not Valid in Single-MSC8101 Mode** **Date Added:** 3/14/2002 **Description:** SDAMUX signal is disabled (stuck at'0')when SDRAM machine handles the memory access and the chip is programmed to single-MSC8101 mode (BCR[EBM]=0). **Workaround:** None. **Fix Plan:** TBD	1K42A

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
SIU16	**Bus Busy Disable Mode Can Hang 60X Bus in Multi-Master Systems** **Date Added:** 5/21/2002 **Description:** The bus busy disable mode (SIUMCR[BBD=1]) can not be used if the MSC8101 is not the only master on the 60X bus. Using this mode in such a system can cause the 60X bus to hang. **Workaround:** 1. If the external master supports the $\overline{\text{ABB}}$ signal, do not use the bus busy disable mode and connect this signal to the MSC8101. The $\overline{\text{DBB}}$ signal can either be connected or can be pulled up. 2. If the external master does not support the $\overline{\text{ABB}}$ signal do one of the following: a. Do not use the bus busy disable mode and generate the $\overline{\text{ABB}}$ signal externally. The $\overline{\text{DBB}}$ signal can either be connected or can be pulled up. The following external $\overline{\text{ABB}}$ implementation should be sufficient to work around the problem: Assert the $\overline{\text{ABB}}$ signal whenever a qualified bus grant for the external master is sampled (Bus grant asserted while $\overline{\text{ARTRY}}$ and $\overline{\text{ABB}}$ are negated). Negate the $\overline{\text{ABB}}$ signal when there is no qualified bus grant. The negation of $\overline{\text{ABB}}$ should be as follows: Drive $\overline{\text{ABB}}$ to VDD for half a clock cycle and then stop driving it (HIGH-Z). b. If using the internal arbiter and up to two external masters, connect the external bus grants (through an AND gate if more than one) to an available external bus request and define the priority for that request to be the highest in the PPC_ALRH register. The $\overline{\text{DBB}}$ signal can either be connected or can be pulled up. **Fix Plan:** TBD	1K42A
SIU18	**ARTRY Assertion When Using Pipeline Depth of Zero** **Date Added:** 10/15/2002 **Description:** Internal (60x) slave maintains a pipeline depth of zero by asserting AACK only after TA. When ARTRY is asserted the 60x bus access will be terminated and TA will not be asserted. Therefore the Internal (60x) slave will not assert AACK since TA was not asserted. **Workaround:** Use a pipeline depth of one (BCR[PLDP]=0) for applications that require memory coherency. **Fix Plan:** TBD	1K42A
SIU19	**Bus Monitor Timeout When Using External Slave** **Date Added:** 10/15/2002 **Description:** When using an external 60x bus slave with the bus monitor activated, PSDVAL is not asserted when the external slave is accessed, which could cause the bus monitor to time-out and TEA to be asserted. **Workaround:** The following workarounds 1. Use pipeline depth of zero (BCR[PLDP]=1) when using an external 60x bus slave. 2. Disable 60X bus monitor, SYPCR[PBME]=0. 3. If the external 60x bus slave is another 810x or 826x device, connect the PSDVAL signals together. **Fix Plan:** TDB	1K42A

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
QSIU3	**TEA May Hang PPC Bus** **Date Added:** 5/30/2000: **Description:** TEA may hang the PPC bus if it is asserted between specific address and data phases during a split transaction. **Workaround:** Enable Bus Monitor. **System Number:** 5724 **Fix Plan:** TBD	1K42A
QSIU4	**Extended Mode on the Local Bus** **Date Added:** 6/13/2000: **Description:** Using Extended mode on the local bus can generate incorrect transactions in certain combinations of consecutive reads and writes. **Workaround:** Do not use Extended mode on the local bus. **System Number:** 5959 **Fix Plan:** Not currently scheduled	1K42A
QSIU5	**Incorrect Data on PowerPC Bus** **Date Added:** 6/13/2000, modified 10/15/2002 **Description:** The following sequence on the PowerPC bus can result in incorrect data: 1. Read transaction with DACK before AACK. 2. Failed atomic write transaction 3. Write transaction **Workaround:** None **System Number:** 5823 **Fix Plan:** RevA	1K42A
QSIU6	**EE[4–5] Pins are Sampled on $\overline{\text{HRESET}}$,$\overline{\text{SRESET}}$ and $\overline{\text{PORESET}}$** **Date Added:** 8/31/2000 **Description:** The EE[4–5] pins should be sampled only on $\overline{\text{PORESET}}$, but they are sampled on $\overline{\text{SRESET}}$ and $\overline{\text{HRESET}}$ as well. Changing the value of the EE[4–5] pins after $\overline{\text{PORESET}}$ negation might prevent the chip from booting, because their value might choose a different or undefined boot configuration. **Workaround:** The EE[4–5] values should be kept constant and equal to the values on $\overline{\text{PORESET}}$. **Fix Plan:** Rev A	1K42A
QSIU7	**Pin $\overline{\text{IRQ7\_INTOUT}}$ Not Open Drain** **Date Added:** 9/6/2000 **Description:** INOUT pin $\overline{\text{IRQ7\_INTOUT}}$ should be open-drain but not implemented as one. **Workaround:** Buffer $\overline{\text{INTOUT}}$ on the board when it is wire ORed. **Fix Plan:** Rev. A	1K42A

Table 2. Silicon Errata (Continued)

<table>
<tr><th>Errata Number</th><th>Errata Description</th><th>Applies to Mask</th></tr>
<tr><td>QSIU12</td><td>Limited Clock Modes
Date Added: 4/2/2001, Modified 2/19/2002
Description: Single-master and Multi-master systems are limited to clock mode 57 for 1K42A and 46 or 57 for 2K42A (see also QSIU14). Note that in mode 46 a 33MHz CLKIN can be used which will result in a 16.5MHz input to the SPLL. Although this is slower than the specified 18MHz (refer to the MSC8101 Data Sheet), this is not an issue in mode 46.

Available 1K42A Clock Modes
<table><tr><th>MODCK</th><th>BUS:CPM:CORE</th><th>BUS:CLKIN</th><th>MAX BUS</th><th>MAX CPM</th><th>MAX CORE</th></tr><tr><td>57</td><td>1:2.5:5</td><td>1.0</td><td>55</td><td>138</td><td>275</td></tr></table>
Fix Plan: Rev A</td><td>1K42A</td></tr>
<tr><td>QSIU13</td><td>Software Watchdog Cannot be Enabled after Boot from Host
Date Added: 8/5/2001
Description: The software watchdog is disabled when booting from host. It cannot be subsequently enabled because the SYPCR can only be written once.
Workaround: None
Fix Plan: Rev A</td><td>1K42A</td></tr>
<tr><td>QSIU14</td><td>Non-Functional DLL
Date Added: 11/25/2001, modified 7/31/2002
Description: DLL may fail to lock.
Workaround: Use DLL disabled mode by setting the DLLDIS bit in the Reset Configuration Word. To maximize bus performance, use a zero-delay buffer for CLKOUT for both single-master and multi-master systems. In multi-master systems the clock master should also be the memory controller.
System Number: 7427
Fix Plan: Rev A</td><td>1K42A</td></tr>
<tr><td>QSIU15</td><td>60x Compatible Global Transaction Fail on RETRY
Date Added: 5/30/2000, modified 10/15/2002
Description: Data may be lost on RETRY when global transactions are performed in 60x compatible mode.
Workaround: When global transactions are used, 60x compatible mode cannot be used.
System Number: 5678
Fix Plan: RevA</td><td>1K42A</td></tr>
<tr><td>QSIU16</td><td>ALE Output During Reset
Date Added: 2/20/2003
Description: ALE behavior is not guaranteed during reset. This affects only multi-master systems which perform reset configuration from external memory and which use ALE for all memory accesses. ALE recovers with the first access after reset.
Workaround: None
System Number:
Fix Plan: RevA</td><td>1K42A</td></tr>
</table>

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
DMA1	**DMA Data Corruption on either PPC Bus or Local Bus** **Date Added:** 2/19/2002 **Description:** Data transferred by the DMA on either the PPC Bus or Local Bus may be corrupted. **Workaround:** For DMA accesses on the PPC Bus - disable PPC bus pipeline by setting BCR[PLDP]=1. For DMA accesses on the Local Bus the UPMC programming patch is available. **System Number:** 7462 **Fix Plan:** RevA	1K42A
EFC1	**Inaccurate EFCOP IIR Outputs For Two or Fewer Coefficients** **Date Added:** 2/19/2002 **Description:** When using normal (dual) DMA or fly-by DMA transfers which have maximum transfer size greater than 32-bits with the EFCOP to perform IIR filtering with two or less IIR coefficients, the first output of IIR filter will be lost. The rest of the outputs will be shifted and inaccurate. Use only DMA 32-bit maximum transfer size for both input and output channels. **Fix Plan:** Not currently scheduled.	1K42A
BOOT1	**Incorrect Checksum for Host Bootload** **Date Added:** 8/15/2000: **Description:** The host bootload calculates erroneous checksum. **Workaround:** Clear ICR[HF3] so that the host bootload ignores the checksum comparison result. **System Number:** 6178 **Fix Plan:** Rev A	1K42A

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask

BOOT2	**Boot Interference in Multi-Master System with Shared Memory**
	Date Added: 8/5/2001
	Description: The DSPRAM address in the memory map as programmed by the boot loader code in the ROM is the same for all processors. During simultaneous boot, this will cause interference of one processor with another.
	Workaround: For up to 4 MSC8101's including the configuration master.
	Boot the processors one after the other, and not at the same time. Reprogram unique DSPRAM address for each processor. The configuration master is set also to be the arbitration master and the memory controller for the system. The configuration word for the master should set the MMR field of the reset word (bits [18:19]) to 2'b11. This will mask all the external bus requests of the configuration slaves. After the master completes its boot, the user should:
	1. Clear all external requestors from the Arbitration Level Register (ALR) of the arbitration master.
	2. Reprogram the UPM of the DSPRAM bank to unique address (see programming example below)
	3. Set priority for the next configuration slave in the Arbitration Level Register (ALR) of the arbitration master.
	4. Enable external bus requests by clearing SIUMCR MMR field (bits [16:17]).
	5. Repeat stages 2,3 for consecutive slaves.
	Configuration master programming code:
	`move.l PPC_ALRH,D7 ; Step #1`
	`move.l PPC_ALRL,D8`
	`bmclr.w #$f,D7.L`
	`bmclr.w #$ff00,D8.H`
	`move.l D7,PPC_ALRH`
	`move.l D8,PPC_ALRL`
	`upmc init $04000000 ; Step #2 (DSPRAM base address $0400_0000)`
	`move.l PPC_ALRH,D7 ; Step #3`
	`nop`
	`bmset.w #$7,D7.L`
	`nop`
	`move.l D7,PPC_ALRH`
	`move.l SIUMCR,D7; Step #4`
	`nop`
	`bmclr.w #$c000,D7.L`
	`nop`
	`move.l D7,SIUMCR`
	Fix Plan: RevA
		1K42A

GEN1	**Device Withstands MM ESD of 75V Instead of 100V** **Date Added:** 5/21/2002 **Description:** Device meets the ESD specifications for Human Body Model (HBM) of 1000V and Charged Device Model (CDM) of 500V but does not withstand the Machine Model (MM) requirement of 100V. All pins guaranteed to withstand 75V MM. **Workaround:** None. **Fix Plan:** RevA	1K42A

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
GEN2	**Unexpected Outputs During Boundary Scan** **Date Added:** 10/18/2002 **Description:** D[32:60] outputs may behave indeterminately during boundary scan. **Workaround:** Reset the device by asserting PORESET while HPE/EE1=0. Alternatively, assert PORESET throughout boundary scan. **Fix Plan:** RevA	1K42A
SC1	**PC Cannot Be Updated in Debug Mode Entered From Asynchronous Interrupt** **Date Added:** 10/5/2000 **Description:** When a DEBUG instruction is executed in a static or dynamic delay slot created by an asynchronous interrupt, the core enters Debug mode, but the PC cannot be updated. **Workaround:** In the dynamic case, the debugger can use a status bit in the ESR, which indicates whether the core entered a debug in a delay slot. Software workarounds are available for all the static cases. A detailed description was sent by StarCore and can be resent upon request. **Fix Plan:** RevA	1K42A
SC3	**Erroneous Trace Buffer Value** **Date Added:** 10/5/2000 **Description:** An erroneous 62-bit value may be written to the trace buffer when the EOnCE is programmed to write both event counters (ECNT_VAL and ECNT_EXT). **Workaround:** None. **Fix Plan:** RevA	1K42A
SC4	**SC140 May Hang After Write To PCTL0 Register.** **Date Added:** 2/19/2002 **Description:** Write to PCTL0 immediately freezes the core for 150-900 cycles. If the system is busy (e.g. pre-fetch transactions), the core may not exit the freeze state. **Workaround:** Option A: 1. Make sure the EFCOP is not working. 2. Make sure the local bus to L1 memory is not working. 3. The program that writes to PCTL0 is in internal memory. 4. Write to PCTL0 immediately after reset before any external data accesses. Option B: Do not write to PCTL0. **System Number:** 7560 **Fix Plan:** TBD	1K42A
SC5	**SC140 CORE May Hang After Illegal Execution Set** **Date Added:** 2/19/2002 **Description:** Upon receipt of an illegal execution set the SC140 CORE may enter a freeze state that can only be released by reset. **Workaround:** No workaround available. **System Number:** 7541 **Fix Plan:** TBD	1K42A

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
SC6	**Incorrect Data on Trace Buffer Read During Core Freeze** **Date Added:** 2/19/2002 **Description:** After writing data to the Trace Buffer, the TB is disabled, in order to read from it. There are 2 options to read the TB and the problem occurs in both: **1.** Reading the TB by software. If, While reading the TB by SW into a core register, there is a core freeze, One data over-write the previous data. **2.** Reading the TB from the JTAG. If the JTAG reads the TB while there is a core freeze, the data will not be correctly sampled. **Workaround:** **1.** Software: Read the TB by software, when there is no core freeze: a. The program will be in internal memory. b. Make sure the EFCOP is not working. c. Make sure the local bus to L1 memory is not working. d. The Write-Buffer is empty. e. There are no other move commands except for the TB read. **2.** JTAG: a. Read the TB from JTAG only when the core is in DEBUG mode. b. Before reading the TB, flush the Write-Buffer. **System Number:** 7604 **Fix Plan:** TBD	1K42A
SC7	**Change of Flow May Cause Incorrect Trace-Buffer Data** **Date Added:** 2/19/2002 **Description:** When programing the EOnCE for tracing events of change of flow (TCHOF) and interrupts (TINT), the Trace-Buffer will be updated on every event by the source and destination addresses. In the event of a CHOF (change of flow) to another CHOF with an interrupt request in between, the Trace-Buffer will be updated with additional data. The additional data is incorrect and is not needed for the trace. **Workaround:** Perform post-processing after reading the Trace-Buffer. Search in the data for a source address and the destination before it should be the destination of that source. That means there is a destination which came before its source. Delete the source and the previous data. 7794 **Fix Plan:** TBD	1K42A
SC8	**Debug Exception Request Form JTAG is Not Accepted During Core Freeze** **Date Added:** 5/21/2002 **Description:** JTAG debug exception request is not accepted by the Core during freeze. If the request is asserted and negated during core freeze, the request will be discarded. **Workaround:** Assert Debug request from JTAG. When entering the exception routine, assert by software an external pin (EE pin for example), to signal the exception Service Routine is now executed. After that, a new JTAG instruction can be written. **Fix Plan:** TBD	1K42A

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
SC9	**EE Pins Do Not Enable Different EOnCE Modules During Core Freeze** **Date Added:** 5/21/2002 **Description:** If EE pins are asserted to enable events in EOnCE during core freeze and the request is negated during the same core freeze, the event is not enabled. **Workaround:** Poll on Core status from JTAG. Assert the EE pin(s) until the Core is not in freeze for at least 3 cycles. **Fix Plan:** TBD	1K42A
CPM2	**CAM Access Not Atomic** **Date Added:** 5/30/2000: **Description:** The bus atomicity mechanism for CAM access may not function correctly when the CPM's DMA accesses the CAM. This only affects systems in which multiple CPMs will access the CAM. **Workaround:** None **System Number:** 1410 **Fix Plan:** Rev A	1K42A
CPM4	**No CTS Lost Indication with HDLC** **Date Added:** 5/30/2000 **Description:** When CTS is negated at the end of HDLC frame, (last flag or one bit before) transmission will be aborted. However there is no CTS-LOST indication. There is only abort indication. **Workaround:** None **System Number:** 1670 **Fix Plan:** Rev A	1K42A
CPM5	**Data Corruption on SDMA Flyby** **Date Added:** 5/30/2000 **Description:** The data of an SDMA write, which follows a SDMA flyby read in the local bus may be corrupted. **Workaround:** None **System Number:** 1720 **Fix Plan:** Rev A	1K42A
CPM6	**Erroneous Report of Overrun on FCC** **Date Added:** 5/30/2000 **Description:** Spurious overrun indications on the FCC may occur in the following cases: 1. After a stop transmit command is issued. 2. Following a CTS lost condition. 3. Late collision under ethernet. **Workaround:** None **System Number:** 1746 **Fix Plan:** Rev A	1K42A
CPM7	**Erroneous Report of Overrun With Fast Ethernet** **Date Added:** 5/30/2000 **Description:** If the CRS (carrier sense) signal is negated while fast ethernet frame is transmitted, an overrun error may occur and the FCC may have to be reset. **Workaround:** None **System Number:** 1752 **Fix Plan:** Rev A	1K42A

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
CPM8	**Error on Transmit On Demand Register** **Date Added:** 5/30/2000 **Description:** The TODR mechanism may freeze serial channels. **Workaround:** Do not use TODR. **System Number:** 2484 **Fix Plan:** Rev A	1K42A
CPM9	**Erroneous Reception of ATM Cell** **Date Added:** 5/30/2000 **Description:** Under certain conditions, an ATM receiver may receive cells of PHYs which were not addressed for it. Details of the condition: • ATM receiver in UTOPIA slave mode. • FIFO full condition occurred (this happens only when the transmitter violates the UTOPIA standard requirements: transmits data without CLAV). • Transmitter changed selected PHY number. • FIFO full condition ended (CPM read some data from FIFO). **Workaround:** Use different VPI/VCI for different PHYs or expect the cells to be discarded by higher-level protocol software. **System Number:** 2493 **Fix Plan:** Rev A	1K42A
CPM10	**Error in ATM Underrun Report** **Date Added:** 5/30/2000 **Description:** In ATM, a Transmit internal rate underrun error is not reported correctly in the TIRU field of the FCCE register. In most cases, TIRU is not set in the FCCE when an internal rate underrun error occurs. In some rare cases that depend on internal sequences within the communications controller, the TIRU bit may be set as expected when the error should be reported. **Workaround:** None **System Number:** 2611 **Fix Plan:** Rev A	1K42A
CPM11	**False Indication of Shared Flag** **Date Added:** 5/30/2000 **Description:** FCC-TX HDLC - FCT_TXD (data out) changes from 1-->0 for 1 ser_clock period, few clocks after the reset command from MAIN is given. A false shared flag can be detected at the receiver if the last bit before reset was 0, and the receiver considers it as a closing flag of the frame. In most of cases, a CRC error is generated and the frame is discarded. **Workaround:** None **System Number:** 3024 **Fix Plan:** Rev A	1K42A
CPM13	**Error in Random Number Generation** **Date Added:** 5/30/2000 **Description:** In Fast Ethernet transmit, when more then one (up to four) frames reside in the FCC FIFO, random number generation (for collision wait) may produce the same number for all four frames. **Workaround:** None **System Number:** 3421 **Fix Plan:** Rev A	1K42A

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
CPM14	**Corruption of ATM Cells** **Date Added:** 5/30/2000 **Description:** Corruption of ATM cells may occur when the following combination is used: AAL1 with UDC in which the user-defined header size is 9 to 12 octets and PM is not used. **Workaround:** Since this problem appears in a very specific condition as described above, avoiding any of the elements (e.g., using cell header of 8 octets) eliminates it. **System Number:** 3488 **Fix Plan:** Rev A	1K42A
CPM15	**Corruption of Port D Registers** **Date Added:** 5/30/2000 **Description:** The PDATA, PDATB, PDATC, and PDATD registers can only be written with a 32-bit write instruction. (i.e., stw). When 8- or 16-bit write instructions (i.e., sth, stb) are used, the bits not being written may be corrupted. **Workaround:** Use a 32-bit write instruction only to write to the PDATA, PDATB, PDATC, and PDATD registers. **System Number:** 3679 **Fix Plan:** Rev A	1K42A
CPM17	**Error in Reporting UTOPIA Error Condition** **Date Added:** 5/30/2000 **Description:** An FCC receiver which is configured as single PHY master does not detect a UTOPIA error condition when SOC and CLAV are not asserted simultaneously. **System Number:** 3728 Rev A	1K42A
CPM21	**False Indication of Collision in Fast Ethernet** **Date Added:** 5/30/2000 **Description:** In the Fast Ethernet a false COL is reported whenever a collision occurs on the preamble of the previous frame. **Workaround:** S/W should ignore COL indications when the CRC of the frame is correct. **System Number:** 3927 **Fix Plan:** Rev A	1K42A
CPM22	**False Defer Indication in Fast Ethernet** **Date Added:** 5/30/2000 **Description:** In the fast ethernet, if a frame is transmitted due to defer and this frame also gets late collision, a false defer indication is indicated for the next frame. **Workaround:** None **System Number:** 3981 **Fix Plan:** Rev A	1K42A
CPM24	**Error in Indicating IDLE Between Frame** **Date Added:** 5/30/2000 **Description:** In the FCC HDLC transmitter, if slow serial clock (cpm_freq/serial_clock > 16) is used, RTS does not transition to IDLE between frames. This means that all the frames are transmitted back-to-back in case there is valid data in the transmitter's FIFO. **Workaround:** None **System Number:** 3998 **Fix Plan:** Rev A	1K42A

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
CPM25	**RTS Not Synchronized to Serial Clock** **Date Added:** 5/30/2000 **Description:** In the FCC HDLC transmitter in nibble mode, the negation of RTS output signal is not synchronized to the serial clock. The RTS is negated after the last nibble of the data and always before the next edge of the serial clock. **Workaround:** None **System Number:** 4089 **Fix Plan:** The errata will not be corrected due to minimal system impact and/or availability of simple work-arounds.	1K42A
CPM27	**Error in Heartbeat Checking in FCC** **Date Added:** 5/30/2000 **Description:** The heartbeat checking in FCC transmit ethernet 10Mbps does not work properly. The standard requires that the collision pulse from the PHY should be checked within a window of 4usec from the falling edge of the carrier sense. The MSC8101 samples the collision signal only once at exactly 4usec (10 serial clocks) after the falling edge of the carrier sense signal. **Workaround:** None **System Number:** 4155 **Fix Plan:** Rev A	1K42A
CPM28	**Error in Receive Frame Threshold** **Date Added:** 5/30/2000 **Description:** In the SCC Rx in HDLC mode, RFTHR does not work. There is no way to get interrupts on the receive side after a programmable number of frames. **Workaround:** RFTHR should be programed to 1. **System Number:** 4163 **Fix Plan:** Rev A	1K42A
CPM29	**MAXD1 and MAXD2 May Not Be Less Than MFLR** **Date Added:** 5/30/2000 **Description:** In SCC Rx ethernet, the option of transferring only part of a frame into memory (MAXD1 and MAXD2 < MFLR) does not work. **Workaround:** None **System Number:** 4166 **Fix Plan:** Rev A	1K42A
CPM30	**Graceful Stop Command Does Not Work** **Date Added:** 5/30/2000 **Description:** The graceful stop command does not work in SCC Tx in the following protocols: Ethernet, HDLC, Transparent. **Workaround:** None **System Number:** 4167 **Fix Plan:** Rev A	1K42A
CPM35	**Data Corruption in SCC Transparent Mode** **Date Added:** 5/30/2000 **Description:** When SCC transparent, envelope mode is used and the received frame size is (4*n) + 1, the last byte is corrupted. When GSMR_H(RFW) - rx FIFO width is used, the received data is completely corrupted, not just the last byte. **Workaround:** The bug can be worked around with a microcode patch. **System Number:** System number; 4350 **Fix Plan:** Rev A	1K42A

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask

CPM36	**SI SYNC Timing Restriction**
	Date Added: 5/30/2000
	Description: SI's sync signal may not change exactly on clock edge in the following cases. The bug affects operation only when the SI is in one of two modes:
	`fsd = 00, ce = 0, fe = 0, dsc=1`
	(Sync sampled with falling edge -> Sync should not change on rising edge)
	`fsd = 00, ce = 1, fe = 1, dsc=1`
	(Sync sampled with rising edge -> Sync should not change on falling edge).
	Workaround: When working in these modes, the sync signal to the SI should be manipulated such that it does not change on the exact edge of the serial clock. Toggle the sync at least 5ns after the edge. One way to implement such a workaround is to add a noninverting buffer between the device that generates the sync signal and the MSC8101 that uses it.
	System Number: 3258
	Fix Plan: Rev A.
		1K42A

CPM38	**Heartbeat Error and Carrier Sense Lost Error On Two Frames** **Date Added:** 5/30/2000 **Description:** There are rare cases when a heartbeat error and carrier sense lost error are reported on two frames. The error is reported in the frame in which it occurred, but in those rare cases it is also reported on an adjacent frame. **Workaround:** None **System Number:** 1547,1550 **Fix Plan:** Rev A	1K42A
CPM39	**Corruption in AAL0 Cell Payload** **Date Added:** 5/30/2000 There is a rare case in using the ATM AAL0 transmitter that the AAL0 cell payload may be corrupted. This can occur in certain internal sequence of events that the user cannot detect or control. 1. Use the available microcode patch from the web site. 2. When working with AAL0 SAR, place the TCELL_TMP_BASE 64 byte align plus 4. For example use TCELL_TMB_BASE = 0x2d04 not 0x2d00. 4648a Rev A	1K42A
CPM40	**Corruption in AAL0 IDLE Cell** **Date Added:** 5/30/2000 There is a rare case when transmitting an ATM idle cell that the idle cell may be corrupted. This can occur in certain internal sequences of events that cannot be controlled or detected by the user. Place the Idle Base template at address 64 byte align minus 4. For example use Idle_BASE = 0x2cfc not 0x2d00. 4648b Rev A	1K42A

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
CPM41	**Limitation in ATM Controller** **Date Added:** 5/30/2000 There are some limitations in the ATM controller. The first limitation is that only the first 8 PM tables can be used instead of 64. When using these 8 tables, the user must clear the 5 most significant bits of TBD_BASE (in case of Tx PM) or RBD_BASE (in case of Rx PM). The second limitation is that only the first 2048 ATM channel numbers can be used. There is a microcode patch that can fix the PM limitation. The ATM channel number limitation has no workaround. 4744 Rev A	1K42A
CPM42	**Data Corruption in MCC** **Date Added:** 5/30/2000 **Description:** Data corruption may occur in the receive buffers of MCC channels when more then one TDM slot uses 7 bits of contiguous data. **Workaround:** It is possible to avoid this problem by splitting the 7 bits slots between two SI ram entries such that one entry will represent 4 bits of the slot and the other SI entry will represent 3 bits of the slot. The errata occurs only when all the 7 bits are represented by one entry in the SI ram. **System Number:** 4743 **Fix Plan:** Rev A	1K42A
CPM43	**TxCLAV Ignored By UTOPIA in Single PHY Mode** **Date Added:** 5/30/2000 **Description:** When the FCC transmitter is configured to work in UTOPIA single PHY master mode, it ignores negation of the TxCLAV signal. Therefore, the UTOPIA slave cannot control the flow of cells by negating TxCLAV. Note that this bug affects Rev A.1 chips only. **Workaround:** Configure the FCC to work in multi-master mode but limit the number of PHYs to 1 by programming: FPSMR[LAST PHY] = 5'b0 **System Number:** 4882 **Fix Plan:** Rev A	1K42A
CPM44	**Zero Insertion Error on MCC** **Date Added:** 5/30/2000 **Description:** When the MCC transmitter is used in HDLC super channel mode, a zero insertion at the last bit before the flag fails to occur. **Workaround:** There is a microcode patch which fixes the problem. **System Number:** 4941 **Fix Plan:** Rev A	1K42A
CPM45	**Error in CLAV Sample Point** **Date Added:** 5/30/2000 **Description:** In FCC ATM transmit master mode (multiple PHY only), the CLAV signal is sampled 5 clocks before the end of the cell instead of 4 clocks. This is relevant only for back-to-back transmission sequence. **Workaround:** In multiple PHY fix priority polling mode, by adding a dummy PHY, it is possible to ensure that the dummy PHY is polled at payload 44 (5 clocks before the end of the cell). This is possible since the cell length is constant and the number of PHY to poll is also constant. **System Number:** 5031 **Fix Plan:** Rev A	1K42A

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
CPM46	**Error in Internal Prioritization of CPM Resource** **Date Added:** 5/30/2000 **Description:** Each of the communication controllers (FCC, MCC, SCC, ...) issues request for service to the CPM with different priorities in order to receive the necessary assistance in time. Because of an internal connection error, the FCC3 request for service is issued with a much lower priority than intended. Because of this, FCC3 may sporadically overrun when the CPM is heavily loaded. **Workaround:** None **System Number:** 5663 **Fix Plan:** Rev A	1K42A
CPM48	**Error in TDM** **Date Added:** 5/30/2000 **Description:** Disabling TDMx may interfere with the operation of TDMy if TDMy uses the SI-RAM blocks directly above those used by TDMx. For example: start address of TDMc = 0 start address of TDMb = 2 start address of TDMd = 4 when disabling TDMd, TDMb is affected. when disabling TDMb, TDMc is affected. when disabling TDMc, No TDM is affected. **Workaround:** Instead of disabling a TDM, the user can switch to a shadow RAM that contains only non supported slots in its entries. **System Number:** 5714 **Fix Plan:** Rev A	1K42A
CPM49	**Error in FEC CAM address recognition** **Date Added:** 3/14/2002 **Description:** External CAM address recognition in Fast Ethernet controller does not function. **Workaround:** Use microcode patch available from Freescale. **System Number:** 5404 **Fix Plan:** RevA	1K42A
CPM50	**MCC Transparent Super Channel Loss of Alignment** **Date Added:** 5/30/2000 **Description:** When the MCC is configured to work in Transparent, super channel first sync slot synchronization, loss of alignment may occur when the first data (idles) on the Rx data line matches the value of the RCVSYNC parameter. **Workaround:** Write to RCVSYNC a pattern which cannot appear in the Rx data line. **System Number:** 5833 **Fix Plan:** Rev A	1K42A

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
CPM54	**Error in switching to and from shadow SI ram.** **Date Added:** 12/10/2000, modified 15/10/2002 **Description:** Dynamic switching in SIRAM may not be executed properly. **Workaround:** In SI RAM, when working with shadow RAM, the last entry (n) and the entry immediately before the last entry (n-1) MUST have at least one common bit in the CNT or BYT fields. For example: SIRAM Entry CNT BYT n-1 000 1 n 010 1 The above is okay n-1 101 0 n 001 0 The above is okay n-1 100 0 n 001 0 The above is not okay. **System Number:** 6282, 6283 **Fix Plan:** RevA	1K42A
CPM55	**Error in ATM_Transmit command.** **Date Added:** 12/10/2000 **Description:** The ATM_Transmit command does not execute correctly when used on APC priority above 4. **Workaround:** None. **System Number:** 6162 **Fix Plan:** Rev A	1K42A
CPM57	**AAL5 Cell Corruption.** **Date Added:** 1/28/2001 **Description:** The second part of a second cell may overwrite the second part of the first cell in an AAL5 frame. **Workaround:** Use microcode patch. **Fix Plan:** Rev A	1K42A
CPM64	**AAL5 RxBD[LNE] error generated if PDU length exceeds 65512 bytes** **Date Added:** 5/31/2001 **Description:** When the CPM receives an AAL5 PDU between 65512-65535 bytes (maximum length) the CPM sets the RxBD[LNE] indicating a receive length error, however the memory buffer contents for the PDU are correct. **Workaround:** Receive AAL5 PDU less than 65512 bytes or use microcode patch. **System Number:** 7025 **Fix Plan:** Rev A	1K42A

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
CPM65	**SS7 Microcode in ROM does not function correctly** **Date Added:** 8/5/2001 **Description:** The SS7 microcode in ROM does not function correctly and should not be used. **Workaround:** Use the Enhanced SS7 microcode package. **Fix Plan:** Rev A	1K42A
CPM71	**CPM does not snoop MCC buffer descriptors.** **Date Added:** 8/5/2001 **Description:** When the MCC performs a DMA read or write of the buffer descriptor, GBL is not asserted and TC2 is always driven low.Therefore cache snooping will not be enabled for MCC BDs, therefore BDs in memory will not match the data cache. Also the bus used for the DMA is always the 60x, therefore if the BDs are on the local bus then the DMA consumes bandwidth on both the 60x and Local bus. **Workaround:** If GBL and/or TC2 are set in the MCC TSTATE/RSTATE parameters, use microcode patch available from Freescale which fixes the above problem. If GBL and TC2 are not set to improve performance move the MCC BDs to the 60x bus. The microcode patch will fix both the GBL/TC2 and the bus performance issue. **System Number:** 7018 **Fix Plan:** Rev A	1K42A
CPM72	**MCC Global Underruns** **Date Added:** 8/5/2001 **Description:** An MCC transmitter global underrun (GUN) error may result from intensive activity on FCC1 (e.g.burst of short back to back Ethernet frames).This is due to the prioritization of the MCC transmitter relative to FCC1 receiver and transmitter as well as the MCC receiver. **Workaround:** Each serial channel above can request a service at normal or emergency level. In case of emergency, the request is handled before normal (non-emergency) request of the channels at a higher priority level.The proposed change is to allow the MCC transmitter to assert an emergency request instead of normal request. The impact on FCC1 in this case is minimal.This feature will controlled by a new MCC mode bit in future MSC8101 revisions. This new MCC mode bit will allow users to continue to use the current CPM priority scheme in their applications if required. **System Number:** **Fix Plan:** RevA	1K42A
CPM73	**SI RAM Corruption** **Date Added:** 8/5/2001 **Description:** (7049)An access to the SI RAM bank from the 60x bus while the corresponding TDM is active may result in data corruption within the SI RAM. **Workaround:** Associate the SI RAM bank with an inactive TDM before attempting to access it. Once the accesses has been made, the SI RAM bank should be re-assigned to the active TDM. **System Number:** 7049 **Fix Plan:** Rev A	1K42A
CPM74	**FCC HDLC Controller Stops Transmitting When Using Nibble Mode With MFF=0** **Date Added:** 8/27/2001 **Description:** When running an FCC in HDLC nibble mode with the multi-frame per FIFO bit off (MFF=0) the CPM may lose synchronization with the FCC HDLC controller. As a result the HDLC controller will get stuck and stop transmission. **Workaround:** When running the FCC in HDLC nibble mode set the MFF=1 or alternatively run the FCC in HDLC bit mode. **Fix Plan:** RevA	1K42A

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
CPM76	**First transmitted bit zero in FCC Transparent Mode with GFMR[CTSS]=1** **Date Added:** 8/27/2001 **Description:** When using an FCC in transparent mode the first bit of a frame is transmitted as zero every time RTS is asserted before CTS is asserted when CTS is sampled synchronously with data (GFMR[CTSS]=1). If CTS is in pulse mode (GFMR[CTSP]=1) only the first frame is affected because CTS is ignored thereafter. If CTS is not in pulse mode (GFMR[CTSP]=0) then every frame is affected separately. **Workaround:** If the receiver synchronizes on a 8/16-bit sync pattern stored in the FDSR register (GFMR[SYNL]=1x) ensure that the synchronization pattern starts with a "0". If no synchronization pattern is used (GRMR[SYNL]=0x) add a one-byte dummy buffer before sending the real data buffers. **Fix Plan:** RevA	1K42A
CPM79	**FCC Fast Ethernet Flow Control** **Date Added:** 3/14/2002 **Description:** When the FCC receives a flow control pause message with MAC parameter =0xffff, it sets a zero delay instead of maximum delay. **Fix Plan:** RevA	1K42A
CPM80	**MCC CES User Template** **Date Added:** 3/14/2002 **Description:** If the transparent MCC Tx CES channel requires the user template (CHAMR[UTM]=1) only the first 8 bytes of the user defined pattern are transmitted. Then the transmitter will continue to send bytes 4-7 of the pattern continuously until the counter reaches 0. Any bytes defined in the pattern after byte 7 are never transmitted. **Workaround:** Use a template size of 8 bytes. **Fix Plan:** RevA	1K42A
CPM85	**Only One BSY Interrupt Generated for AAL0** **Date Added:** 5/21/2002 **Description:** When using AAL0, only one BSY interrupt will be received regardless of the number of BSY events that are generated. **Workaround:** None. **Fix Plan:** RevA	1K42A
CPM86	**Random PHY Number For FCC RX in Single-PHY Master Mode** **Date Added:** 5/21/2002 **Description:** When the FCC Receive ATM controller is configured for Single PHY Master mode (FPSMR[RUMP]=0, FPSMR[RUMS]=0) and FPSMR [LAST PHY / PHY ID] is not equal to zero, a random PHY ID might be allocated to the incoming cells instead of the expected zero (for Single-PHY). This will result in a loss of cells. This configuration is typical when using the FCC Transmit ATM controller in Multi-PHY Master mode together with the FCC Receive ATM controller in Single PHY Master mode. **Workaround:** The Address Lookup Mechanism should be created in such a way that for any PHY Addr input, the Output will be as for PHY 0. **Fix Plan:** RevA	1K42A

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
CPM88	**MCC Transmit GUN when MCC STOP RX CPCR Command is used** **Date Added:** 10/15/2002 **Description:** An MCC may experience a highly intermittent transmit GUN event indication, related to MCC receive channels that have been stopped via the MCC STOP RX host CPCR command. This GUN can happen unrelated to internal CPM loading or other external factors. **Workaround:** Avoid using MCC STOP RX command using one of the following mechanisms: **1.** Simply stop the TDM or **2.** Use shadow RAM and dynamically remove the desired MCC RX channel entry from SIRAM programming (see 8101 Reference Manual chapter 20). The following procedure should be utilized, using an extra redundant shadow RAM switch. This is done to provide a full TDM frame's amount of time to ensure receive activity is complete and will avoid the issue: a. Re-program shadow SIRAM to remove channel to be stopped. b. Switch to shadow SIRAM and wait for that TDM's bit in the SIxSTR register to change to indicate switch complete. c. Copy this new shadow RAM programming back to the main SIRAM bank. d. Switch to active RAM, again wait for switch to complete. e. Then software can re-initialize or modify the removed channel's RX parameters. **System Number:** 2905 **Fix Plan:** RevA	1K42A
CPM95	**ATM False Indication of Mis-Inserted Cells** **Date Added:** 2/25/2003 **Description:** There is a false indication of unassigned bits in the PHY:VPI:VCI which could cause ATM cells to be treated as mis-inserted cells and therefore be discarded. **Workaround:** Use microcode patch available from Freescale. **Fix Plan:** RevA	1K42A
CPM96	**ATM Performance Monitoring with AAL1 CES** **Date Added:** 2/25/2003 **Description:** ATM Performance Monitoring with AAL1 CES Data in DPRAM is corrupted when performance monitoring is enabled in the receiver. **Workaround:** Implement one of the following: **1.** Disable Receive Performance Monitoring RCT[PMT]=0. **2.** Use microcode patch available from Freescale. **Fix Plan:** TBD	1K42A

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
CPM98	**I^2C Erratic Behavior Can Occur if Extra Clock Pulse is Detected on SCL** **Date Added:** 8/25/2003 **Description:** The I^2C controller has an internal counter that counts the number of bits sent. This counter is reset when the I2C controller detects a START condition. When an extra SCL clock pulse is inserted between transactions (before START and after STOP conditions), the internal counter may not get reset correctly. This could generate partial frames (less than 8 bits) in the next transaction. **Workaround:** Do not generate extra SCL pulses on the I^2C bus. In a noisy environment, the digital filter I2MOD[FLT] and additional filtering capacitors should be used on SCL to eliminate clock spikes that may be misinterpreted as clock pulses. **System Number:** MSIls09133 **Fix Plan:**	1K42A
CPM99	**CPM 99: ABR TCTE[ER-TA] Corruption** **Date Added:** 8/25/2003 **Description:** When the AAL5 ABR ROM microcode is in use, the TCTE[ER-TA] field can be overwritten with an erroneous value. This, in turn, causes the TCTE[ER-BRM] to be updated with this value. Because TCTE[ER-BRM] holds the maximum explicit rate value allowed for B-RM cells, an erroneous value in this field could have a detrimental effect on the network performance. **Workaround:** Use the microcode patch available from Freescale	1K42A
CPM100	**CPM 100: ABR TCTE Address Miscalculation** **Date Added:** 8/25/2003 **Description:** When using the AAL5 ABR ROM microcode with external ATM channels it is possible for the EXT_TCTE_BASE word value (written by the user to DPRAM) to be misread. In this case calculations performed by the microcode to access the users programmed external TCTE will be incorrect with a high chance of the access resulting in a CPM crash. **Workaround:** Use the microcode patch available from Freescale. **System Number:** MSIls09131 **Fix Plan:**	1K42A

Table 2. Silicon Errata (Continued)

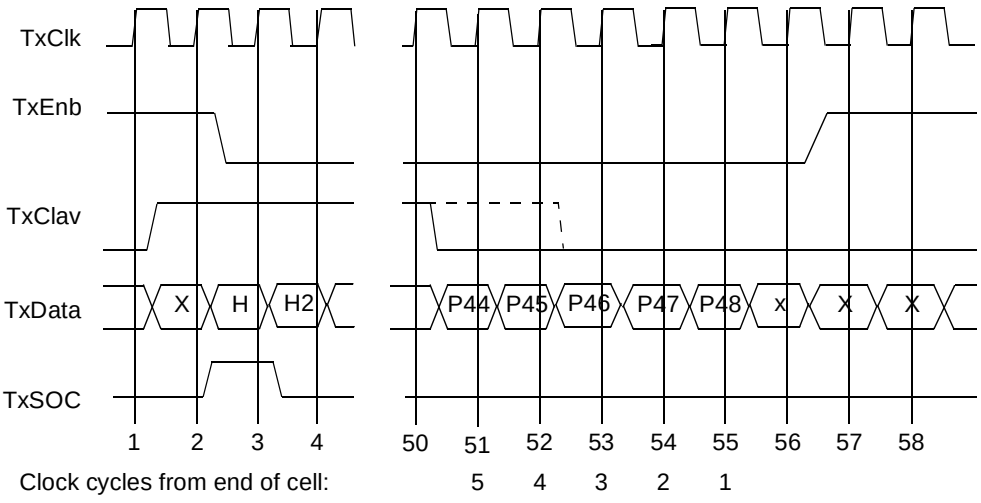
Errata Number	Errata Description	Applies to Mask
CPM101	**FCC RxClav Timing Violation (Slave)** **Date Added:** 1/15/2004 **Date Revised:** 11/05/2004 **Description:** FCC ATM Receive UTOPIA slave mode. When the RxFIFO is full, RxClav is negated 2 cycles before the end of the cell transfer, instead of 4. A master that polls RxClav or pauses 3 or 4 cycles before the end of the cell transfer may sample a false RxClav, and an overrun condition may occur. The dashed line in the timing diagram below depicts the actual RxClav negation (two cycles before the end of the cell transfer instead of four cycles). The signals in the timing diagram are with respect to the master, so the Tx interface is shown. **Workaround:** 1. The master should not poll RxClav or pause a cell transfer 4 cycles before the end of a cell transfer. The master should poll 2 cycles before the end of the current cell or later. This can be achieved by introducing cell-to-cell polling (and transfer) delay, which is equal or larger than one cell transfer time. If this can be achieved, the impact on performance is minimal. 2. Configuring ATM only on FCC1 and setting FPSMR[TPRI] ensures the highest priority to FCC1 Rx. In addition, for CPM usage lower then 80 percent (as reported by the CPM performance tool based on UTOPIA maximal bus rate), the CPM performance is enough to guarantee that the RxFIFO does not fill up.  	1K42A
CPM110	**FCC1 Prioritization** **Date Added:** 12/19/2003 **Description:** The FCC1 receiver in Ethernet, HDLC, or Transparent controller mode is not elevated to emergency status (priority 4 in Table 19-2 of the Reference Manual, "Peripheral Prioritization"), which may lead to a FIFO overrun if the system is heavily loaded (FCC1 receiver has the highest priority excluding emergency status of other peripherals). **Workaround:** When allocating FCCs, assign FCC2 and FCC3 for Ethernet, HDLC or Transparent before FCC1, or assign FCC1 to the lowest bit rate interface. If FCC1 is allocated for ATM and requires higher CPM usage than the other FCCs, disable its emergency status. **System Number:** 11062 **Fix Plan:**	1K42A

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
CPM111	**FCC Missing Reset** **Date Added:** 1/15/2004 **Description:** The TxBD may not close for the FCC in Half-Duplex 10BaseT Ethernet. There may be a mismatch between the actual transmitted BD and the BD for which the status is updated. As a result, the status of one to three BDs may not be updated. They appear to be “ready” although the associated frames have been transmitted (assuming a frame per BD). **Workaround:** Use microcode patch provided by Freescale. **System Number:** 11064 **Fix Plan:**	1K42A
CPM112	**FCC Missing Reset at OverRun** **Date Added:** 12/19/2003 **Description:** TxBD may not be closed for FCC in Half-duplex 10BaseT Ethernet. There may be a mismatch between the actual transmitted BD and the BD for which status is updated. As a result, the status of one to three BDs may not be updated, and they would appear "Ready", although the associated frames have been transmitted (assuming a frame per BD). **Workaround:** Use microcode patch provided by Freescale. **System Number:** 11064, 11067 **Fix Plan:** N/A	1K42A
CPM113	**Incorrect Return Value from Event Register Read (SCC, SPI, I^2C, and SMC)** **Date Added:** 12/19/2003 **Description:** When the Event Register is read while the SCC, SPI, I^2C, or SMC is active, it is sometimes read as 0, even though it has some bits set. **Workaround:** **System Number:** 11068 **Fix Plan:**	1K42A
CPM115	**APC Transmits Unwanted Idle Cells** **Date Added:** 12/19/2003 **Description:** In heavily loaded ATM applications, if the ATM pace controller (APC) is configured for multiple priority levels and a burst of traffic for transmission is sustained long enough on the highest priority APC table, then an unwanted idle cell can be trasmitted on the lower priority APC tables when there are cells available in lower priority APC scheduling table for transmission. The transmission of the unwanted idles could cause the valid ATM cells on lower-priority APC scheduling tables not to be transmitted. This transmission of unwanted idles can affect all ATM channels that are not located in the highest-priority APC scheduling table. **Workaround:** Increase the size of lower-priority APC scheduling tables so they are large enough to absorb any burst or back-to-back bursts on the highest-priority APC scheduling table. Otherwise, use the microcode patch available from Freescale. **System Number:** 11069 **Fix Plan:**	1K42A
CPM116	**Pointer 93 in Partially Filled (PFM) Mode** **Date Added:** 1/15/2004 **Description:** In PFM mode, the pointer value of 93 is not generated, causing the loss of synchronization at the far end. Also, when the pointer value of 93 is received, the synchronization is lost, which causes a loss of data and the resynchronization routine. **Workaround:** Use microcode patch provided by Freescale. **System Number:** 11912 **Fix Plan:**	1K42A

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
QCPM2	**Switched External Clocks For Timers 3,4** **Date Added:** 8/31/2000 **Description:** Internal connectivity between TIN3 and TIN4 is switched. **Workaround:** To work with external clock for timer3 use TIN4, and to work with timer4 us TIN 4. Please note that for timer4 using external clock (TIN3) and TOUT4 is impossible. **System Number:** 6219 **Fix Plan:** Rev0.1	1K42A
CPM117	**False Address Compression** **Date Added:** 11/05/2004 **Description:** If there are active AAL0 channels and a CRC-10 error has been received, VP-level address compression might have false results, which could lead to one of the following: • Wrong calculation of a VP pointer address • Cells might be falsely discarded as misinserted cells • Misidentification of misinserted cells (in CUAB mode) This is a statistical error, which is conditional on the reception of AAL0 cells with a CRC-10 error. The probability of false address compression is directly correlated with higher CPM bit rate and longer system bus latency. While the false address compression is possible only if there are active AAL0 channels, it may have an impact on all AAL types. However, it cannot occur unless AAL0 cells with CRC-10 error have been received beforehand. **Workaround:** Use the microcode patch supplied by Freescale. **System Number:** 17129	1K42A
CPM118	**Aborted HDLC Frame Followed by a Good Frame** **Date Added:** 7/11/2004 **Description:** When an aborted HDLC frame is followed by a good frame, the receive data buffer may contain the data of the aborted frame followed by the data of the good frame. **Workaround:** Use the microcode patch provided by Motorola. **System Number:** 15906 **Fix Plan:**	1K42A
CPM119	**Ethernet Collision Occurs on the Line 125 Clocks after TX_EN Assertion** **Date Added:** 7/11/2004 **Description:** When an ethernet collision occurs on the line 125 clocks after TX_EN assertion, late collision will be reported even though this is only 63 bytes into the frame instead of 64. When a collision occurs 124 cycles after TX_EN assertion, no event is reported, the TxBD is not closed, and transmission halts. Retransmission behavior is correct for collisions occurring between assertion of TX_EN and 123 clocks. **Workaround:** Use the microcode patch provided by Motorola. **System Number:** 15908 **Fix Plan:**	1K42A

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
CPM120	**SS7_OPT[FISU_PAD] parameter has no effect on the number of flags between FISUs** **Date Added:** 12/22/2004 **Description:** The SS7_OPT[FISU_PAD] parameter has no effect on the number of flags between FISUs. Regardless of the value of this field, one flag will be present between back-to-back FISUs. **Workaround:** Use the latest SS7 microcode package provided by Freescale. **System Number:** 18767 **Fix Plan:** None at this time.	1K42A
CPM121	**TDM Data Frame Corruption** **Date Added:** 11/05/2004 **Description:** During a write to one of the SI registers (GMR, AMR, BMR, CMR, DMR) while one or more TDMs are working, one data frame of a working TDM may become corrupted. **Workaround:** Work with the shadow RAM when changing data and do not disable and then enable the TDM. **System Number:** 17460	1K42A

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