MSE908AP64_2M25D
Rev. 0, 1/2007

Mask Set Errata for Mask 2M25D

Introduction

This mask set errata applies to the mask 2M25D for these products:

- MC68HC908AP64
- MC68HC908AP32
- MC68HC908AP16
- MC68HC908AP8

MCU Device Mask Set Identification

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 2M25D. All standard devices are marked with a mask set number and a date code.

SPI Slave Mode Operation Issue

SE122-SPI-slave

Description

This errata describes a voltage and noise sensitivity issue with the SPI while in slave mode. The SPI, while in slave mode, can experience transmission errors resulting in simultaneous receive and transmit errors. This is attributed to noise corrupting the slave clock input to the SPI module.

Workaround

You must use fault-tolerant software and/or hardware handshaking protocol that can detect errant data and request re-transmission of the data from the SPI master. The SPI master in-turn must be able to detect anomalous data from the slave SPI and request re-transmission of the data from the SPI slave.

NOTE:

Use of the SPI in slave mode at a nominal voltage of 3.3 V virtually eliminates the issue. All designs should incorporate decoupling capacitors very close to the MCU to avoid noise injection from the application.

Brief Pause on Standard Input/Output Pins during Power-On-Reset

SE95-I/O_POR

Description

During a power-on-reset, a brief pulse may appear on the following I/O pins: PTA0-PTA7, PTB4-PTB7, PTC0-PTC5, and PTD0-PTD7. The brief pulse, which is due to the turn-on delay of the internal regulator, can drive active-high output circuits (for example, relays or NPN transistors) momentarily. The turn-on delay is greater for slow rising VDD supplies. Input circuits are not affected.

Workaround

Add an external RC filter to the output port pin, where necessary, for control sensitive applications.

In applications where these brief pulses could cause undesirable effects, add an external RC filter between the MCU output pin and the circuit that it drives.

FLASH Memory Erasing and Programming

SE71-FLASH

To maintain data integrity in the FLASH memory, do not access FLASH memory locations that are not intended for program or erase once the high voltage enable bit is set (HVEN = 1). If the COP is enabled, a COP counter reset (write to $FFFF) should be performed before setting the HVEN bit.

FLASH Page Erase Operation

Do not access any other FLASH locations between steps 4 to 8.
Do not reset the COP counter between steps 4 to 8.

1. Set the ERASE bit and clear the MASS bit in the FLASH control register.
2. Write any data to any FLASH location within the page address range desired.
3. Wait for a time, t_{nvs} (5 μs).
4. Set the HVEN bit.
5. Wait for a time t_{erase} (20 ms).
6. Clear the ERASE bit.
7. Wait for a time, t_{nvh} (5 μs).
8. Clear the HVEN bit.
9. After time, t_{rcv} (1 μs), the memory can be accessed in read mode again.

FLASH Program Operation

Do not access any FLASH locations that are not intended for programming between steps 4 to 11. Do not reset the COP counter between steps 4 to 11.

1. Set the PGM bit. This configures the memory for program operation and enables the latching of address and data for programming.
2. Write any data to any FLASH location within the address range of the row to be programmed.
3. Wait for a time, t_{nvs} (5 μs).
4. Set the HVEN bit.
5. Wait for a time, t_{pgs} (10 μs).
6. Write data to the FLASH location to be programmed.
7. Wait for time, t_{prog} (20 μs to 40 μs).
8. Repeat steps 6 and 7 until all bytes within the row are programmed.
9. Clear the PGM bit.
10. Wait for time, t_{nvh} (5 μs).
11. Clear the HVEN bit.
12. After time, t_{rcv} (1 μs), the memory can be accessed in read mode again.

ADC Accuracy at Zero Volt Input

SE68-ADC

The 10-bit ADC conversion result for 0V input (zero input reading) is $000, $001, $002, or $003; not the specified $00 or $01. With inputs of 5mV and above, the ADC is within the specified accuracy of ±1.5 LSB (see **Figure 1**).

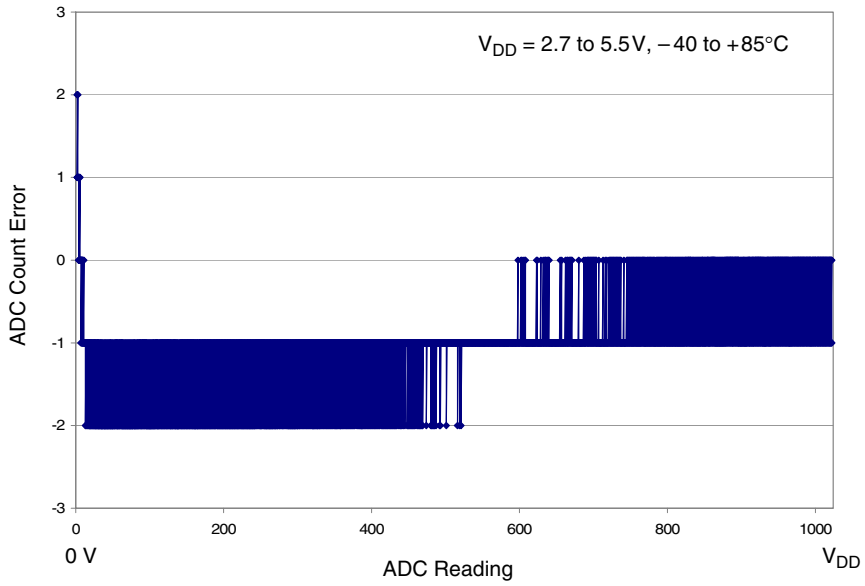

Figure 1. Typical ADC Error Count

Low-Voltage Inhibit Reset in Stop Mode

SE67-LVI

An internal reset occurs when entering stop mode if the LVI control bits are configured as shown in the table below:

CONFIG1 Register ($001F)			
Bit 4	Bit 3	Bit 6	Bit 5
LVIPWRD	LVIREGD	LVISTOP	LVIRSTD
X	X	0	0
1	1	X	

X = don't care
LVIPWRD=1 is V_{DD} LVI circuit disabled.
LVIREGD=1 is V_{REG} LVI circuit disabled.
LVISTOP=0 is LVI disabled in stop mode.
LVIRSTD=0 is LVI resets enabled.

To enter stop mode with LVI disabled, set LVIRSTD=1 before entering stop mode. This will not cause an internal reset and also reduces the stop I_{DD} to a minimum.