Mask Set Errata for Mask 1M40J

Introduction

This report applies to mask 1M40J for these products:
- MC9S08QE8

MCU device mask set identification

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 0J27F. All standard devices are marked with a mask set number and a date code.

MCU device date codes

Device markings indicate the week of manufacture and the mask set used. The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code "0301" indicates the first week of the year 2003.

MCU device part number prefixes

Some MCU samples and devices are marked with an SC, PC, or XC prefix. An SC prefix denotes special/custom device. A PC prefix indicates a prototype device which has undergone basic testing only. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC or SC prefix.

SE184-FLVD-STOP3: False low voltage detect when exiting stop3

Errata type: Silicon

Affected component: SoC level behavior

Description: If the low voltage detect (LVD) is enabled (LVDE = 1) but not in stop mode (LVDSE = 0), on some devices the low voltage detect flag (LVDF) will occasionally be set when exiting stop3 mode. If the LVD interrupt is enabled (LVDIE = 1) the interrupt vector will be fetched. If the LVD reset is enabled, the part will reset, and the LVD bit in the System Reset Status (SRS) register will be set. The correct operation of the device is to wake and execute the code immediately after the STOP instruction.

If the LVD is not enabled (LVDE = 0) or if LVD is also enabled during stop mode (LVDSE = 1) then this issue will not occur. If the LVD is enabled during stop mode the stop3 current will increase.

Workaround: A software level change to reliably eliminate the issue is to use only the LVD interrupt (LVDE = 1, LVDIE = 1, and LVDRE = 0). Inside the LVD interrupt service routine, a short state of health check can be made to verify the supply level before proceeding. In this routine, the LVDF should be cleared and then read to determine whether a true low voltage event is present. If the LVDF is set when it is read, then a true LVD condition exists and the MCU can be reset by forcing the execution of an illegal op-code.

SE157-ADC-INCORRECT-DATA: Boundary case may result in incorrect data being read in 10- and 12-bit modes

Errata type: Silicon

Affected component: ADC

Description: In normal 10-bit or 12-bit operation of the ADC, the coherency mechanism will freeze the conversion data such that when the high byte of data is read, the low byte of data is frozen, ensuring that the high and low bytes represent result data from the same conversion.

In the errata case, there is a single-cylce (bus clock) window per conversion cycle when a high byte may be read on the same cycle that subsequent a conversion is completing. Although extremely rare due to the precise timing required, in this case, it is possible that the data transfer occurs, and the low byte read may be from the most recently completed conversion.

In systems where the ADC is running off the bus clock, and the data is read immediately upon completion of the conversion, the errata will not occur. Also, in single conversion mode, if the data is read prior to starting a new conversion, then the errata will not occur.

The errata does not impact 8-bit operation.

Introducing significant delay between the conversion completion and reading the data, while a following conversion is executing/pending, could increase the probability for the errata to occur. Nested interrupts, significant differences between the bus clock and the ADC clock , and not handling the result register reads consecutively, can increase the delay and therefore the probability of the errata occuring.

Workaround: Using the device in 8-bit mode will eliminate the possibility of the errata occuring.

Using the ADC in single conversion mode, and reading the data register prior to initiating a subsequent conversion will eliminate the possibility of the errata occuring.

Minimizing the delay between conversion complete and processing the data can minimize the risk of the errata occuring. Disabling interrupts on higher priority modules and avoiding nested interrupts can reduce possible contentions that may delay the time from completing a conversion and handling the data. Additionally, increasing the bus frequency when running the ADC off the asynchronous clock, may reduce the delay from conversion complete to handling of the data.

SE156-ADC-COCO: COCO bit may not get cleared when ADCSC1 is written to

Errata type: Silicon

Affected component: ADC

Description: If an ADC conversion is near completion when the ADC Status and Control 1 Register (ADCSC1) is written to (i.e., to change channels), it is possible for the conversion to complete, setting the COCO bit, before the write instruction is fully executed. In this scenario, the write may not clear the COCO bit, and the data in the ADC Result register (ADCR) will be that of the recently completed conversion.

If interrupts are enabled, then the interrupt vector will be taken immediately following the write to the ADCSC1 register.

Workaround: It is recommended when writing to the ADCSC1 to change channels or stop continuous conversion, that you write to the register twice. The first time should be to turn the ADC off and disable interrupts, and the second should be to select the mode/channel and re-enable the interrupts.

SE149-PMC: High I_{DD} upon entering stop3 mode after exiting stop3 mode using external reset

Errata type: Silicon

Affected component: PMC

Description:

Description: Scenario 1

Following a power-on event, the first time the MCU enters stop3 with the LVD configured to be disabled in stop3 mode, the LVD circuitry is correctly disabled and the device exhibits expected I_{DD}s. When stop3 mode is exited via assertion of external reset, a subsequent entry to stop3 may result in a high current state due to the LVD being enabled even though LVDE and LVDSE configure LVD to be disabled in stop3 mode. Exit from stop3 from any source corrects the failing logic and results in normal Stop3 currents on following entries to stop3.

When only external reset is used to wake the device from Stop3, the operation alternates between the LVD on and LVD off condition during stop3 with each external pin reset.

Scenario 1, Example A

- Device goes through POR, and application code runs and enters stop3. -> Typical stop3 I_{DD} observed.

- Pin RESET is used to exit stop3, and application code runs and reenters stop3 -> Elevated stop3 I_{DD} observed.
- Pin RESET is again used to exit stop3, and application code runs and reenters stop3 -> Typical stop3 I_{DD} observed.
- Pin RESET is again used to exit stop3, and application code runs and reenters stop3 -> Elevated stop3 I_{DD} observed.
- Stop3 is exited using any other source except Reset pin –> Typical stop3 I_{DD} observed.
- etc.

Scenario 1, Example B

- Device goes through POR, and application code runs and enters stop3. -> Typical stop3 I_{DD} observed.
- Pin RESET is used to exit stop3, and application code runs and reenters stop3 -> Elevated stop3 I_{DD} observed.
- Stop3 is exited using any other source except Reset pin –> Typical stop3 I_{DD} observed.

Description: Scenario 2

Another way for the errata behavior to be seen is when both stop3 with LVD disabled and stop3 with LVD enabled are used in the same application. If a device is configured to enter stop3 with LVD enabled at some point in the application, and an LVD Reset occurs while in stop3, elevated I_{DD}s will be seen on the next stop3 entry, whether the LVDE and LVDSE bits are then cleared or set, disabling or enabling the LVD, respectively.

Workaround: Either of the following are potential workarounds.

- Do not use a external pin reset to wake up from stop3. Use another method to wake from stop3; for instance: a KBI or IRQ input to perform the external pin wakeup function.
- Write code to enable RTI or ADC to wakeup after entering stop3; enter stop3 ; wake from stop3 on RTI or ADC complete; then reenter stop3 with RTI or ADC disabled. You would use the ADC to spend the least amount of time in the high current mode.

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