

Mask Set Errata for Mask 0N22G / 0P80C

This report applies to mask 0N22G / 0P80C for these products:

- MC9S12ZVL32
- MC9S12ZVL16
- MC9S12ZVL8
- MC9S12ZVLS32
- MC9S12ZVLS16

Table 1. Errata and Information Summary

| Erratum ID | Erratum Title |
|------------|--|
| ERR006181 | ADC: ADCSTS[RVL_SEL] is not changed as specified in rare corner case if ADC disabled while flow control request SEQA ongoing |
| ERR006975 | ADC: Conversion Command List (CSL) swapping not consistent in corner case of Restart and LoadOK overrun scenario |
| ERR006964 | ADC: Flag RSTAR{EIF is set unexpectedly in corner cases |
| ERR006965 | ADC: Flag TRIG{EIF not set if erroneous TRIG request occurs short before STOP Mode entry or WAIT Mode entry with bit SWAI set |
| ERR008188 | ADC: High current in Stop Mode |
| ERR006866 | ADC: Maximum number of commands 63 instead of 64 |
| ERR007019 | FTMRZ: Problem with Flash commands 'Set User Margin Level' and 'Set Field Margin Level' |
| ERR006167 | S12Z_BDC: OVRUN bit is set unexpectedly after GO_UNTIL command (ACK enabled) |
| ERR006131 | S12Z_BDC: SYNC_PC during STOP (without clocks) causes setting of OVRUN flag |
| ERR006722 | S12Z_BDC: WRITE_MEM, FILL_MEM commands issued during STOP with the core clock disabled can write incorrect data to the addressed location. |
| ERR008346 | SCI: RXEDGIF interrupt miss while enter STOP |



Table 2. Revision History

| Revision | Changes |
|---------------|---|
| 05 DEC 2014 | Initial revision |
| March 11 2021 | The following errata were added. <ul style="list-style-type: none">• ERR006866• ERR008346 The following erratum was revised. <ul style="list-style-type: none">• ERR008188 |

ERR006181: ADC: ADCSTS[RVL_SEL] is not changed as specified in rare corner case if ADC disabled while flow control request SEQA ongoing

Description: In case a Sequence Abort Request is in process (ongoing) and the ADC gets disabled (ADCEN = 1'b0) before:

The Sequence Abort Request is finished which terminates any possible ongoing data bus access to store a conversion result.

In this case the RVL select is not changed as specified. Instead it is unchanged.

Workaround: The ADC should not be disabled before any flow control request (SEQA, TRIG, RSTA) is finished (all flow control bits are cleared).

It is recommended to issue a Sequence Abort Request and to poll bit SEQA to be clear before ADC is disabled via bit ADCEN.

ERR006975: ADC: Conversion Command List (CSL) swapping not consistent in corner case of Restart and LoadOK overrun scenario

Description: The CSL list swapping is not consistent when the conditions below are true:

- The CSL is configured for double buffer mode
- A Restart Event is in process (Conversion Command of a CSL is loaded)
- Then a Restart Request/LoadOK overrun situation happens just within a few cycles (previous Restart Request not finished)
- While the current CSL is aborted, an additional Restart Request/LoadOK overrun situation occurs

Expected behavior description:

If Restart/LoadOK overrun situations occur, then those requests should be stored in the background. So each Restart Request overrun with LoadOK should swap the selected/tracked CSL into the background. The ongoing list should be aborted and the last selected/tracked CSL must be started.

Error behavior description:

In the current case the second Restart Event overrun with LoadOK actually misses the LoadOk and the selected/tracked CSL is not swapped in the background. This leads to differently used command lists between modules e.g. for devices with PTU, the PTU and ADC command lists are no longer in sync.

Single Restart Request overruns with LoadOK within a few cycles after the previous Restart Request are tracked correctly.

NOTE:

A single Restart/LoadOK overrun scenario can happen in a motor control application, but not a multiple overrun situation within a few cycles.

Workaround: If possible, avoid multiple Restart Request overrun scenarios.

ERR006964: ADC: Flag RSTAR{EIF is set unexpectedly in corner cases

Description: In case of repeated Restart Request overruns (Restart overrun occurs again before previous Restart overrun could be handled) the RSTAR{EIF is erroneously set if:

- The first Restart Request overrun occurs correctly with a simultaneous Sequence Abort Request AND
- The second Restart Request overrun occurs without Sequence Abort Request, which is a flow control failure but for overrun situation the issue should not be flagged.

Misbehavior:

The ADC flags the flow control failure (RSTAR{EIF bit is set) in the second overrun which should not happen. Overruns are tracked quietly and executed as soon as Sequence Abort turnaround time allows.

Workaround: If possible, avoid multiple Restart Request overrun scenarios.

ERR006965: ADC: Flag TRIG{EIF not set if erroneous TRIG request occurs short before STOP Mode entry or WAIT Mode entry with bit SWAI set

Description: At Low power Mode entry (STOP or WAIT with bit SWAI set) all current flow control information as well as all pending flow control information gets deleted immediately.

In case of a flow control error, the detection can take several cycles until it is flagged by TRIG{EIF.

This leads to the corner case in which TRIG{EIF does not get set because the device enters STOP or WAIT with SWAI set .

Workaround: The ADC should be idle (no conversion or conversion sequence or Command Sequence List ongoing) when entering STOP mode or WAIT with bit SWAI set.

ERR008188: ADC: High current in Stop Mode

Description: The ADC can take a higher current in Stop Mode (500µA increasing over time to about 1mA per ADC instance) if the ADC is enabled and conversions have been done.

There is a software workaround available.

Workaround: This software workaround has been validated.

The subroutine ADC0_stop_current_workaround takes about 105 bus clock cycles (ECLK) on S12ZVM128.

The subroutine must be executed for each ADC instance performing conversions before Stop Mode entry.

Before the workaround subroutine is executed, the ADC must be initialized (command list pointers and result list pointers have valid addresses).

Please note:

- All the conversion commands of List 0 must be valid (no illegal channel, no illegal SMP value)
- ADCFMT[SRES] value must not be illegal
- The command fetch must not cause an illegal access flag

```
void main(void) {
...
DisableInterrupts; // Shutdown sequence is not interruptible until STOP
...
ADC0_stop_current_workaround(); // Subroutine must be executed with interrupt protection
asm(andcc #0x6f); /* CCW settings: S = 0, I = 0 */ asm(stop); /* MCU enters Stop mode if S =
0 in CCW */ ... }

//Workaround to avoid ADC high current during STOP mode
//ADC will be disabled in this function
//Therefore following register are cleared:
//Address | Register | Description
//-----+-----+-----
//0x02 | ADCSTS | CSL_SEL, RVL_SEL will be restored at the end of the function
//0x08 | ADCEIF | Error interrupt flags
//0x09 | ADCIF | Interrupt flags (SEQAD_IF, CONIF_OIF)
//0x0C-0x0D:| ADCCONIF | Conversion interrupt flags, EOL (end of list) interrupt flag
//0x0E-0x0F:| ADCIMDRI | Intermediate result information (must be stored by the customer
before,
// | | if this information is still needed after the function execution)
//0x10 | ADCEOLRI | EOL result information (must be stored by the customer before,
// | | if this information is still needed after the function execution)
//0x1C | ADCCIDX |
//0x20 | ADCRIDX |
void ADC0_stop_current_workaround (void) {
byte tmp_ADCxCTL_0 = ADC0CTL_0; // Save customer settings, these values will be restored
afterwards byte tmp_ADCxTIM = ADC0TIM; byte tmp_ADCxSTS = ADC0STS; ADC0CTL_0 =
0x00; // Disable ADC ADC0TIM = 0x00; // ADC is set to maximum frequency // Device
specification of allowed frequency is ignored, // the ADC conversion is stopped when reaching
```

```
error state // There is no conversion result generated. ADC0CTL_0 = 0x88; // ADC is enabled,
single access mode data bus, restart mode ADC0CTL_0 = 0x88; // Re-do in order to
guarantee ADC is ready for requests before Restart Event occurs ADC0FLWCTL = 0x20; //
ADC is restarted, RSTA bit is set: the first command of list 0 is // loaded from memory. The
command type does not matter, the conversion // is immediately stopped while
(ADC0FLWCTL_RSTA == 1) {} // Wait for restart completion (within a few clock cycles)
ADC0FLWCTL = 0x40; // Start conversion (TRIG) ADC0FLWCTL = 0x40; // The second TRIG
immediately generates a TRIG_EIF, ERROR state is entered while (ADC0EIF_TRIG_EIF ==
0) {} // Wait for trigger error interrupt flag (within a few clock cycles) ADC0CTL_0_ADC_SR =
1; // Execute ADC soft-reset (SR), ADC enters IDLE state while (ADC0STS_READY == 0) {} //
Wait for ADC soft-reset done (within a few clock cycles) ADC0CTL_0 = 0x00; // ADC is
disabled ADC0TIM = tmp_ADCxTIM; //Restore previous customer settings ADC0STS =
tmp_ADCxSTS; ADC0CTL_0 = tmp_ADCxCTL_0; // ADC0CTL_0 is the last one to be
restored, in case ADC was enabled before... }
```

ERR006866: ADC: Maximum number of commands 63 instead of 64

Description: According to the specification the maximum number of conversion commands is 64. The implementation supports up to 63 conversion commands.

Workaround: Use 63 conversion commands maximum.

ERR007019: FTMRZ: Problem with Flash commands 'Set User Margin Level' and 'Set Field Margin Level'

Description: When commands 'Set User Margin Level' and/or 'Set Field Margin Level' are executed targeting P-Flash, configured to return to the normal read level (FCCOB2=0, thus effectively disabling any margin level settings previously applied to Flash reads), the margin level is deactivated correctly but execution of further commands on EEPROM is compromised: concurrent reads to P-Flash while an EEPROM command is executed might result in corrupted data being read, and the EEPROM commands might not execute properly with status flags indicating that errors might have occurred.

If any of the commands 'Set User Margin Level' or 'Set Field Margin Level' run on EEPROM (enabling and/or disabling the margin levels) there is no issue.

Workaround: The way to properly restore the functionality is to run 'Set User Margin Level' or 'Set Field Margin Level' to return to the normal read level (FCCOB2=0) loading an EEPROM address in FCCOB0 / FCCOB1, even if at the beginning of the procedure a P-Flash address was used to set the margin level.

ERR006167: S12Z_BDC: OVRUN bit is set unexpectedly after GO_UNTIL command (ACK enabled)

Description: When the GO_UNTIL command with ACK enabled is executed, and BDC is not in active BDM mode, then the ILLCMD flag is set as specified.

But the command following GO_UNTIL sets the OVRUN flag, which is unexpected.

This is not a normal use case because GO_UNTIL is not an active BDM command.

Workaround: Use the SYNC pulse to clear OVRUN.

Development tool vendors can ensure the debugger does not allow GO_UNTIL unless the device is in active BDM.

ERR006131: S12Z_BDC: SYNC_PC during STOP (without clocks) causes setting of OVRUN flag

Description: The OVRUN flag can be set if the debugger host attempts SYNC_PC in Stop mode with the core clock disabled.

This only occurs if the device does not leave Stop mode before SYNC_PC has ended.

This would typically happen if ACK pulses are enabled and the host debugger waits for the ACK pulse until the device leaves Stop mode.

Workaround: Use a SYNC pulse to clear OVRUN

OR

Set BDCCIS so that the core clock remains active during Stop mode

ERR006722: S12Z_BDC: WRITE_MEM, FILL_MEM commands issued during STOP with the core clock disabled can write incorrect data to the addressed location.

Description: With the device core clock disabled during STOP mode debugging (BDCCIS=0) then WRITE_MEM and FILL_MEM commands can cause incorrect data to be written to the addressed location. This can happen if the device leaves STOP mode during execution of the WRITE_MEM, FILL_MEM command.

Workaround: Three workarounds are proposed. The appropriate workaround depends on the individual debugging requirements.

1. Do not disable the device core clock when debugging through STOP (set BDCCIS).

2. If BDCCIS=0 then only use WRITE_MEM, FILL_MEM whilst in active BDM (rather than during code execution).

3. If BDCCIS=0 then use WRITE_MEM.WS/FILL_MEM.WS which indicate that STOP mode occurred. If STOP=1 then read data back to verify correct write execution.

OR Use ACK and then check BDCCSR if a long ACK occurs. If STOP=1 then read data back to verify.

Note that the data could have been overwritten by execution code because the device has since left STOP mode. This is only of use if the user can be sure that the application code does not write to the same location.

ERR008346: SCI: RXEDGIF interrupt miss while enter STOP

Description: If an active edge (falling if RXPOL=0, rising if RXPOL=1) on the RXD input occurs shortly after the execution of the STOP instruction the RXEDGIF is not asserted and the CPU is not woken up. The time window in during which the edge is missed starts about 10 bus cycles after the STOP instruction and is 2-3 bus cycles wide.

Workaround: (1) If more than one edge with a minimum distance of 4 bus cycles occur, the 2nd edge will wake up the CPU. This is the case for instance in a LIN bus system. “The Wake Up Signal consists of a dominant pulse minimum 250 microseconds and maximum 5 milliseconds in length, and it may be sent by any LIN node.”

(2) Use the API to enforce a periodic wake up and check the level of the LIN input.

(3) Reduce the likelihood of occurrence by increasing the bus frequency.

How to Reach Us:**Home Page:**nxp.com**Web Support:**nxp.com/support

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

While NXP has implemented advanced security features, all products may be subject to unidentified vulnerabilities. Customers are responsible for the design and operation of their applications and products to reduce the effect of these vulnerabilities on customer's applications and products, and NXP accepts no liability for any vulnerability that is discovered. Customers should implement appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, COOLFLUX, EMBRACE, GREENCHIP, HITAG, I2C BUS, ICODE, JCOP, LIFE VIBES, MIFARE, MIFARE CLASSIC, MIFARE DESFire, MIFARE PLUS, MIFARE FLEX, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE, MIGLO, NTAG, ROADLINK, SMARTLX, SMARTMX, STARPLUG, TOPFET, TRENCHMOS, UCODE, Freescale, the Freescale logo, AltiVec, C-5, CodeTEST, CodeWarrior, ColdFire, ColdFire+, C-Ware, the Energy Efficient Solutions logo, Kinetis, Layerscape, MagniV, mobileGT, PEG, PowerQUICC, Processor Expert, QorIQ, QorIQ Qonverge, Ready Play, SafeAssure, the SafeAssure logo, StarCore, Symphony, VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine, SMARTMOS, Tower, TurboLink, and UMEMS are trademarks of NXP B.V. All other product or service names are the property of their respective owners. AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro, μ Vision, Versatile are trademarks or registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.

© 2021 NXP B.V.

