1G58E errata
8 Feb 96

This document lists the known bugs in the 1G58E mask set of the MC68328 DragonBall microprocessor.

Rev 1.0
6 Dec 95 Initial release
Rev 2.0
15 Dec 95 Added SPIS bug description (9)
Rev 3.0
2 Jan 96 Clarified Errata 8.
1. Interrupt clear function for Edge Trigger interrupts.
2. Polarity select and Edge Trigger select bits swapped.
Rev 3.1
3 Jan 96 Clarified Errata 8 description of bit-swap.
Rev 3.2
18 Jan 96 Added Timer capture bug description (10).
Rev 3.3
8 Feb 96 Added TXPOL bit read bug description (11).

1. PC5_DTACKB cannot be used as an I/O.

Explanation: While PC5_DTACKB is programmed as an I/O pin, the internal DTACKB signal is permanently asserted. This causes all access to become 0-wait state regardless of the settings in the chip select registers.
Solution: Leave PC5_DTACKB bit in the default state.

2. First clock pulse after wakeup sometimes is a "runt".

Explanation: Depending on the phase of CLK32 when the wakeup signal occurs, the first CLKO pulse is shorter than normal. Experiments indicate that occasionally the processor does not respond to wakeup events.
Solution: Set SYSCLKSEL bits in PLL Control Register ($fff202) to divide by 4 (001) before entering sleep. Immediately after wakeup event restore SYSCLKSEL to divide by 1 (100).

3. Chip does not respond to RESET reliably.

Explanation: The logic equations for the PLL wakeup function do not include RESET in the correct term. As a result, if a reset signal occurs while the chip is asleep, the chip will not respond and will remain asleep.
Solution: For initial power-up, apply power before asserting RESETB. If the chip is asleep, wake the chip up before asserting RESETB.

4. IRQEN bit in PWM Control Register does not function.

Explanation: Bit 14 in the PWM Control Register ($fff500) does not function. The PWM interrupt is always enabled.
Solution: Disable PWM interrupts by setting Bit 7 in the Interrupt Mask Register ($fff306). Disable PWM wakeup events by clearing Bit 7 in the Interrupt Wakeup Enable Register ($fff30a).

5. Real Time Clock does not generate an interrupt on alarm compare while the chip is sleeping or dozing.

Explanation: A logic error in the Real Time Clock circuitry causes alarm events, while sleeping or dozing, to be ignored.
Solution: Utilize the 1 Minute interrupt to trigger time keeping and alarm functions in software.

6. Real Time Clock provides incorrect values when updates occur while CPU clock is inactive (CPU sleeping).

Explanation: The Real Time Clock keeps accurate time however, when updates occur (1 second "tick"), the read buffer register is updated only when the CPU clock is active (not sleep or doze mode). This means that if the clock is read only in response to a Real Time Clock wakeup event, the time value read will be incorrect.
Solution: Utilize the 1 Minute or 1 Second interrupt to trigger time keeping functions in software.

7. Real Time Clock continues to keep time while the RTC Enable bit (bit 7) ($fffboc) is clear.

Explanation: This is not a bug. The Real Time Clock always operates. However The RTC
NOTE: The Real Time Clock does not respond to reset. Upon initial power up, the value in the Hours, Minutes and Seconds register will be random.

8. Clear control bits for edge mode interrupts are reversed.

Explanation: In edge mode the Interrupt Status Register ($fff30c) clear function nibble is bit-rever
Solution: To clear interrupt (only while configured as edge interrupts) the following is required:

IRQ6 ($fff30c bit 19) write 1 to bit 16 (IRQ1 in the data manual) to clear.
IRQ3 ($fff30c bit 18) write 1 to bit 17 (IRQ2 in the manual) to clear.
IRQ2 ($fff30c bit 17) write 1 to bit 18 (IRQ3 in the manual) to clear.
IRQ1 ($fff30c bit 16) write 1 to bit 19 (IRQ6 in the manual) to clear.

8a. Manual has Polarity and Edge Trigger bits swapped (page 2-9)

The manual incorrectly has the Polarity control and Edge Trigger control bits in the Interrupt Control Register ($fff302) swapped. The manual should read:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POL1	POL2	POL3	POL6	ET1	ET2	ET3	ET6	UNUSED							

Address: $(FF)FFF302 Reset Value: 0000

9. SPI-Slave does not receive data reliably.

Explanation: The SPIS module indicates that it has data ready for reading before an 8-bit transfer is complete. Disabling the module does not clear the error and resynchronize the shift register.

Solution: The SPIS module can be emulated in software for data rates slower than 20 kbps.

10. Timer capture edge feature does not operate reliably.

Explanation: The capture-on-edge of the two general purpose timers will not reliably generate an interrupt or latch a counter value in the capture register.

Solution: This feature will be fixed in revision 3G58E.

11. Reading the TXPOL bit returns the value of the RXPOL bit.

Explanation: The TXPOL bit in the UART miscellaneous register (Base + $908, bit 2) does not return the value written to the bit, rather the value of the adjacent bit, RXPOL (bit 3).

Solution: The actual value of the TXPOL bit is the value written to the TXPOL bit. The value read is the value of the RXPOL bit. The function of TXPOL is not affected. Also, the RXPOL bit or it's function is not affected.