General-purpose solution with a rich feature set for audio and video applications

The 56800E core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and microcontroller (MCU) applications. The instruction set is also highly efficient for C compilers, enabling rapid development of optimized control applications.

Target Applications
- Full duplex feature phones
- IP phones
- Client-side IP applications
- Intelligent access devices
- Voice and audio processing
- Voice recognition and command
- General-purpose devices
- Hands-free automotive devices

Overview
The 56858 core offers a rich feature set and on-chip memory interface. It includes external memory expansion with up to 4 MB program or up to 16 MB data addressing space, and is available in both 144-pin LQFP and 144-pin MAPBGA packages. The 56858 core includes 80 KB of on-chip program SRAM and 48 KB of on-chip data SRAM. With two enhanced synchronous serial interfaces (ESSI) this device can provide outputs for 5.1-channel surround sound. The 56858 core is ideal for client-side telecom/datacom applications requiring up to four channels, including IP phones. This device can be designed into multiprocessor systems to provide speech processing, stand-alone Internet audio and hands-free automotive device functionality.

56800E Core Features
- Efficient 16-bit digital signal controller engine with dual Harvard architecture
- 120 MIPS at 120 MHz core frequency
- Single-cycle 16 x 16-bit parallel multiplier-accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- 16-bit bidirectional shifter
- Parallel instruction set with unique addressing modes
- Hardware DO and REP loops
- Three internal address buses and one external address bus
- Four internal data buses and one external data bus
- Instruction set supports both DSP and controller functions
- Four hardware interrupt levels
- Five software interrupt levels
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/enhanced on-chip emulation (EOnCE) debug programming interface

Freescale Technology

DSP56858

<table>
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<tr>
<th>COP/Watchdog</th>
<th>Ext. Memory I/F</th>
<th>6-ch. DMA</th>
<th>Prog. Chip Selects</th>
<th>Up to 47 GPIO</th>
<th>16-bit Quad Timer</th>
<th>Time of Day</th>
<th>PLL</th>
<th>JTAG/EOnCE</th>
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<tr>
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<td>Program Memory</td>
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<td>80 KB SRAM</td>
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<td>2 KB Boot ROM</td>
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</table>

Freescale Technology
Benefits

- Easy to program with flexible application development tools
- Supports multiple processor connections
- 16-bit quad timer module (with four external pins) that allows capture/compare functionality and can be cascaded
- Quad timer module can also be used for simple digital-to-analog conversion functionality
- ESSI with enhanced network and audio modes
- Time of day (TOD) modules for applications requiring clock display
- Flexible 6-channel direct memory access (DMA) allows both internal and external memory transfers with almost no CPU interruption
- Serial peripheral interface (SPI) with master and slave mode supporting connection to other processors or serial memory devices
- Two ESSIs with three transmitters per module provide support for 5.1-channel surround sound

Energy Information

- Fabricated in high-density CMOS with 3.3V, TTL-compatible digital inputs
- Wait and stop modes available

56858 16-bit Digital Signal Processors

- 120 MIPS at 120 MHz
- 80 KB program SRAM
- 48 KB data SRAM
- 2 KB boot ROM
- Access up to 4 MB words of program memory or up to 16 MB data memory
- Chip select logic for glueless interface to ROM and SRAM
- Six independent channels of DMA
- Two ESSIs
- Two serial communications interfaces (SCIs)
- SPI
- 8-bit parallel host interface
- General-purpose 16-bit quad timer
- JTAG/EOnCE for unobtrusive, real-time debugging

56858 Memory Features

- Harvard architecture permits up to three simultaneous accesses to program and data memory
- On-chip memory
  - 80 KB program RAM
  - 48 KB data RAM
  - 2 KB boot ROM
- Chip select logic used as GPIO

56858 Peripheral Circuit Features

- General-purpose 16-bit quad timer
- Two SCIs*
- SPI*
- Two ESSI modules*
- Computer operating properly (COP)/watchdog timer
- JTAG/EOnCE for unobtrusive, real-time debugging

66458 Memory Features

- Six independent channels of DMA
- 8-bit parallel host interface*
- TOD
- 144-pin LQFP and 144-pin MAPBGA packages
- Up to 47 GPIO pins

*Each peripheral I/O can be used alternately as a GPIO..

Award-Winning Development Environment

- Processor Expert technology provides a rapid application design (RAD) tool that combines easy-to-use, component-based software application creation with an expert knowledge system.
- The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigating, compiling and debugging. A comprehensive set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, Processor Expert technology, the CodeWarrior tool suite and EVMs create a comprehensive, scalable tools solution for easy, fast and efficient development.

Product Documentation

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<thead>
<tr>
<th>Product</th>
<th>Order Number</th>
<th>Description</th>
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<tr>
<td>DSP56800E Reference Manual</td>
<td>DSP56800ERM</td>
<td>Detailed description of the 56800E architecture, 16-bit DSP core processor and the instruction set</td>
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<tr>
<td>DSP5685x User’s Manual</td>
<td>DSP5685xUM</td>
<td>Detailed description of memory, peripherals and interfaces of the 56853, 56854, 56855, 56867 and 56885</td>
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<td>DSP56858 Technical Data Sheet</td>
<td>DSP56858</td>
<td>Electrical and timing specifications, pin descriptions and package descriptions</td>
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<tr>
<td>DSP56858 Product Brief</td>
<td>DSP56858PB</td>
<td>Summary description and block diagram of the core, memory, peripherals and interfaces</td>
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Ordering Information

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