Overview
The 56F827 is a member of the 56800 core-based family of digital signal controllers. It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller (MCU) with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility and compact program code, the 56F802 is well-suited for many applications. The 56800 core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

Target Applications
- Noise suppression
- ID tag readers
- Sonic/subsonic detectors
- Security access devices
- Remote metering
- Sonic alarms
- General-purpose devices

Overview
The 56F827 is a member of the 56800 core-based family of digital signal controllers. It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller (MCU) with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility and compact program code, the 56F802 is well-suited for many applications. The 56800 core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

56800E Core Features

<table>
<thead>
<tr>
<th>Benefits</th>
<th>56800E Core Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>&gt; Low-power applications supported by multiple operating modes</td>
<td>&gt; Efficient 16-bit 56800 family digital signal controller engine with dual Harvard architecture</td>
</tr>
<tr>
<td>&gt; Flash memory is engineered to provide reliable, nonvolatile memory storage, eliminating the need for external storage devices</td>
<td>&gt; As many as 40 MIPS at 80 MHz core frequency</td>
</tr>
<tr>
<td>&gt; Easy to program with flexible application development tools</td>
<td>&gt; Single-cycle 16 x 16-bit parallel multiplier-accumulator (MAC)</td>
</tr>
<tr>
<td>&gt; Optimized for C compiler efficiency</td>
<td>&gt; Two 36-bit accumulators, including extension bits</td>
</tr>
<tr>
<td>&gt; Simple updating of Flash memory through serial peripheral interface (SPI), serial communications interface (SCI) or OnCE, using on-chip boot loader</td>
<td>&gt; 16-bit bidirectional shifter</td>
</tr>
<tr>
<td>&gt; Simple interface with other asynchronous serial communication devices and off-chip EE memory</td>
<td>&gt; Parallel instruction set with unique addressing modes</td>
</tr>
<tr>
<td>&gt; Digital-to-analog converter (DAC) functionality available by using quad timer</td>
<td>&gt; Hardware DO and REP loops</td>
</tr>
<tr>
<td>&gt; Sophisticated debugging using OnCE to view core, peripheral and memory contents</td>
<td>&gt; Three internal address buses and one external address bus</td>
</tr>
<tr>
<td>&gt; Analog-to-digital converter (ADC) shut-down mode for power savings</td>
<td>&gt; Four internal data buses and one external data bus</td>
</tr>
<tr>
<td>&gt; Program chip selects allow for enabling/disabling external memory and external peripherals</td>
<td>&gt; Instruction set supports both DSP and controller functions</td>
</tr>
<tr>
<td>&gt; Software subroutine and interrupt stack with depth limited only by memory</td>
<td>&gt; Controller-style addressing modes and instructions for compact code</td>
</tr>
<tr>
<td>&gt; JTAG/on-chip emulation (OnCE™) debug programming interface</td>
<td>&gt; Efficient C compiler and local variable support</td>
</tr>
<tr>
<td>&gt; Simple interface with other asynchronous serial communication devices and off-chip EE memory</td>
<td>&gt; Digital-to-analog converter (DAC) functionality available by using quad timer</td>
</tr>
<tr>
<td>&gt; Sophisticated debugging using OnCE to view core, peripheral and memory contents</td>
<td>&gt; Analog-to-digital converter (ADC) shut-down mode for power savings</td>
</tr>
<tr>
<td>&gt; Program chip selects allow for enabling/disabling external memory and external peripherals</td>
<td>&gt; Software subroutine and interrupt stack with depth limited only by memory</td>
</tr>
</tbody>
</table>

Energy Information
- Fabricated in high-density CMOS with 5V-tolerant, TTL-compatible digital inputs
- Dual power supply, 3.3V and 2.5V
- Wait and multiple stop modes available
**56F827 16-bit Digital Signal Controller**
- Up to 40 MIPS at 80 MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- Hardware DO and REP loops
- 134 KB On-chip Flash
  - 126 KB Program Flash
  - 8 KB Data Flash
  - Boot via Program Flash
- 2 KB Program RAM
- 8 KB Data RAM
- Up to 128 KB external memory expansion each for program and data memory
- JTAG/OnCE for debugging
- General-purpose quad timer
- MCU-friendly instruction set supports both DSP and controller functions: MAC, bit manipulation unit, 14 addressing modes
- 10-channel, 12-bit ADC
- Synchronous serial interface (SSI)
- Up to two SPIs
- Up to three SCIs
- Time-of-day (TOD) timer
- 128-pin LQFP package
- 16 dedicated and 48 shared general-purpose input/outputs (GPIOs) pins

**56F827 Memory Features**
- Harvard architecture permits as many as three simultaneous accesses to program and data memory
- On-chip memory including a low-cost, high-volume Flash solution
  - 134 KB On-chip Flash
  - 126 KB Program Flash
  - 8 KB Data Flash
  - Boot via Program Flash
  - 2 KB Program RAM
  - 8 KB Data RAM
- Off-chip memory expansion capabilities
  - As much as 128 KB data memory
  - As much as 128 KB program memory

**56F827 Peripheral Circuit Features**
- One 10-channel, 12-bit ADC
- General-purpose quad timer
- Three SCIs
- Two SPIs
- SSI
- Four programmable chip selects
- 16 dedicated and 48 multiplexed GPIO pins
- Computer operating properly (COP)/watchdog timer
- Two external interrupt pins
- External reset pin for hardware reset
- JTAG/OnCE for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase-Lock Loop (PLL)-based frequency synthesizer
- One TOD Timer

---

**Product Documentation**
- DSP56800 Family Manual: Detailed description of the 56800 family architecture and 16-bit DSP core processor and the instruction set
  - Order Number: DSP56800FM
- DSP56F826/827 User’s Manual: Detailed description of memory, peripherals and interfaces of the 56F826/827
  - Order Number: DSP56F826-827UM
- DSP56F827 Technical Data Sheet: Electrical and timing specifications, pin descriptions and package descriptions
  - Order Number: DSP56F827
- DSP56F827 Product Brief: Summary description and block diagram of the core, memory, peripherals and interfaces
  - Order Number: DSP56F827PB

---

**Ordering Information**
- Part: DSP56F827
- Supply Voltage: 2.25V–2.75V/3.0V–3.6V
- Package Type: Low-Profile Quad Flat Pack (LQFP)
- Pin Count: 128
- Frequency (MHz): 80
- Order Number: DSP56F827FG80

---

**Award-Winning Development Environment**
- Processor Expert™ (PE) technology provides a rapid application design (RAD) tool that combines easy-to-use, component-based software application creation with an expert knowledge system.
- The CodeWarrior™ Integrated Development Environment (IDE) is a sophisticated tool for code navigating, compiling and debugging. A comprehensive set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE technology, the CodeWarrior tool suite and EVMs create a comprehensive, scalable tools solution for easy, fast and efficient development.

Learn More: For more information about Freescale products, please visit www.freescale.com.