Several features of the NXP 88MW320/322 SoC enable low system costs and high WLAN protocol processing. For example, the high degree of integration in the SoC requires only one 3.3 V power input, a 38.4 MHz crystal and SPI flash, while the RF path needs only a low-pass filter for antenna connection.

Proven and mature IEEE 802.11n/g/b NXP technology powers a full-featured WLAN subsystem in the SoC. This WLAN subsystem integrates a WLAN MAC, baseband, and direct-conversion RF radio with integrated PA, LINA and transmit/receive switch. It also integrates a CPU subsystem with integrated memory to run NXP WLAN firmware to handle real-time WLAN protocol processing to offload many WLAN functions from the main application CPU.

An Arm® Cortex®-M4F CPU that operates up to 200 MHz powers the 88MW320/322 application subsystem. The device supports an integrated 512 KB SRAM, 128 KB mask ROM and a QSPI interface to external flash. An integrated flash controller with a 32 KB SRAM cache enables execute in place (XIP) support for firmware from flash.

The SoC is designed for low-power operation and includes several low-power states and fast wake-up times. Multiple power domains and clocks can be individually shut down to save power. The SoC also has a high-efficiency internal PA that can be operated in low-power mode to save power. The microcontroller and WLAN subsystems can be placed into low-power states, independently, supporting a variety of application use cases. An internal DC-DC regulator provides the 1.8 V rail for the WLAN subsystem.

The SoC provides a full array of peripheral interfaces including SSP/SPI/I²S (3x), UART (3x), I²C (2x), general-purpose timers and PWM, ADC, DAC, analog comparator, and GPIOs. It also includes a hardware cryptographic engine, RTC, and watchdog timer.

The 88MW322 SoC includes a high-speed USB On-The-Go (OTG) interface to enable USB audio, video and other applications.

A complete set of digital and analog interfaces enables direct interfacing for I/O and avoids the need for external chips. The application CPU can be used to support custom application development and avoids the need for another microcontroller or processor.
Figure 1 shows an overall block diagram of the device.

**APPLICATIONS**
- Smart Home—smart outlet, light switch, security camera, thermostat, sprinkler controller, sensor, door lock, door bell, garage door, security system
- Industrial—building automation, smart lighting, Wi-Fi to other radio bridge, point of sale (POS) terminals
- Smart Devices—coffee pot, rice cooker, vacuum cleaner, air purifier, pet monitor, weighing scale, glucometer, blood pressure monitor, fitness equipment
- Smart Appliances—refrigerator, washer, dryer, oven range, microwave, dishwasher, water heater, air conditioner
- Smart Accessories—smart speakers, headset, alarm clock, gaming accessory, remote control
- Gateways—Bluetooth Smart Mesh and other radios to Wi-Fi/IP network

**KEY FEATURES**
- Highly integrated SoC requiring very few external components for a full system operation
- Multiple low-power modes and fast wake-up times
- Full-featured, single stream 802.11n/g/b WLAN

**POWER MANAGEMENT**
- Power modes—active, idle, standby, sleep, shutoff, power-down
- Integrated high-efficiency buck DC-DC converter
- Independent power domains
- Brown-out detection
- Integrated POR
- Wake-up through dedicated GPIO, IRQ, and RTC

**88MW322**—88-pin QFN, 10 x 10 mm
- USB OTG supported
- 50 GPIOs
- 4 GPTs

**TEMPERATURE**
- Commercial: 0° to 70° C
- Extended: -30° to 85° C
- Industrial: -40° to 105° C
- Storage: -55° to 125° C

**WIRELESS**
- IEEE 802.11n/g/b, 1 x 1 SISO 2.4 GHz and HT20
- Integrated CPU, memory, MAC, DSSS/OFDM baseband, direct conversion RF radio, encryption

**TABLE 1: PACKAGE FEATURE DIFFERENCES**

<table>
<thead>
<tr>
<th>Features</th>
<th>68-Pin</th>
<th>88-Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO</td>
<td>35 total GPIO_0 to GPIO_10, GPIO_16, GPIO_22 to GPIO_33, GPIO_39 to GPIO_49</td>
<td>50 total GPIO_0 to GPIO_49</td>
</tr>
<tr>
<td>USB 2.0 OTG</td>
<td>—</td>
<td>1</td>
</tr>
<tr>
<td>GPT</td>
<td>2</td>
<td>4</td>
</tr>
</tbody>
</table>

1 All I/O features are muxed on GPIOs, except WLAN RF TX/RX, USB, reference clock, and reset functionality.
Antenna diversity
- CMOS and low-swing sine wave input clock
- Low-power with deep sleep and standby modes
- Pre-regulated supplies
- Integrated T/R switch, PA, and LNA
- Optional 802.11n features
- One-time programmable (OTP) memory to eliminate need for external EEPROM

WLAN Rx Path
- Direct conversion architecture eliminates need for external SAW filter
- On-chip gain selectable LNA with optimized noise figure and power consumption
- High dynamic range AGC function in receive mode

WLAN Tx Path
- Integrated PA with power control
- Optimized Tx gain distribution for linearity and noise performance

WLAN Local Oscillator
- Fractional-N for multiple reference clock support
- Fine channel step

WLAN Encryption
- WEP 64- and 128-bit encryption with hardware TKIP processing (WPA)
- AES-CCMP hardware implementation as part of 802.11i security standard (WPA2)
- Enhanced AES engine performance
- AES-Cipher-Based Message Authentication Code (CMAC) as part of the 802.11w security standard

WLAN Authentication and Privacy Infrastructure (WAPI)

IEEE 802.11 Standards
- 802.11 data rates of 1 and 2 Mbit/s
- 802.11b data rates of 5.5 and 11 Mbit/s
- 802.11g data rates 6, 9, 12, 18, 24, 36, 48, and 54 Mbit/s for multimedia content transmission
- 802.11g/b performance enhancements
- 802.11n compliant with maximum data rates up to 72.2 Mbit/s (20 MHz channel)
- 802.11d international roaming
- 802.11e quality of service
- 802.11h transmit power control
- 802.11i enhanced security
- 802.11k radio resource measurement extension
- 802.11n block acknowledgment extension
- 802.11r fast hand-off for AP roaming
- 802.11w protected management frames
- Fully supports clients (stations) implementing IEEE Power Save mode
- Wi-Fi direct connectivity

MICROPROCESSOR

Processor
- Arm Cortex-M4F, 32-bit
- 200 MHz main bus clock

Memory
- 128 KB ROM
- 512 KB RAM

Flash Controller
- Supports QSPI flash devices
- Memory-mapped access to QSPI flash devices
- 32 KB SRAM cache

Digital Interfaces
- 3 x I²S stereo
- 3 x SPI master/slave
- 2 x I²C master/slave
- 3 x UART
- 1 x USB OTG 2.0, high-speed
- 1 x QSPI
- Up to 50 GPIOs
- 2 x wake-up pins

Analog
- 2-step ADC with integrated PGA and configurable resolution/speed
  - 12-bit/2 MHz sample(s) for fast conversion
  - 16-bit/16 kHz sample/s with voice quality
  - 8 single channels or 4 differential channels
- 2-channel or 1 differential channel DAC, 10-bit/500 ksps
- 2 analog comparators with programmable speed/current
- On-die/off-chip temperature sensing and battery monitor

Counters/Timers/PWM
- General-purpose timers (GPT) with LED PWM support
- Real-time clock (RTC)
- CM4 system tick
- Watchdog timer