68K/ColdFire V2 Core Architecture

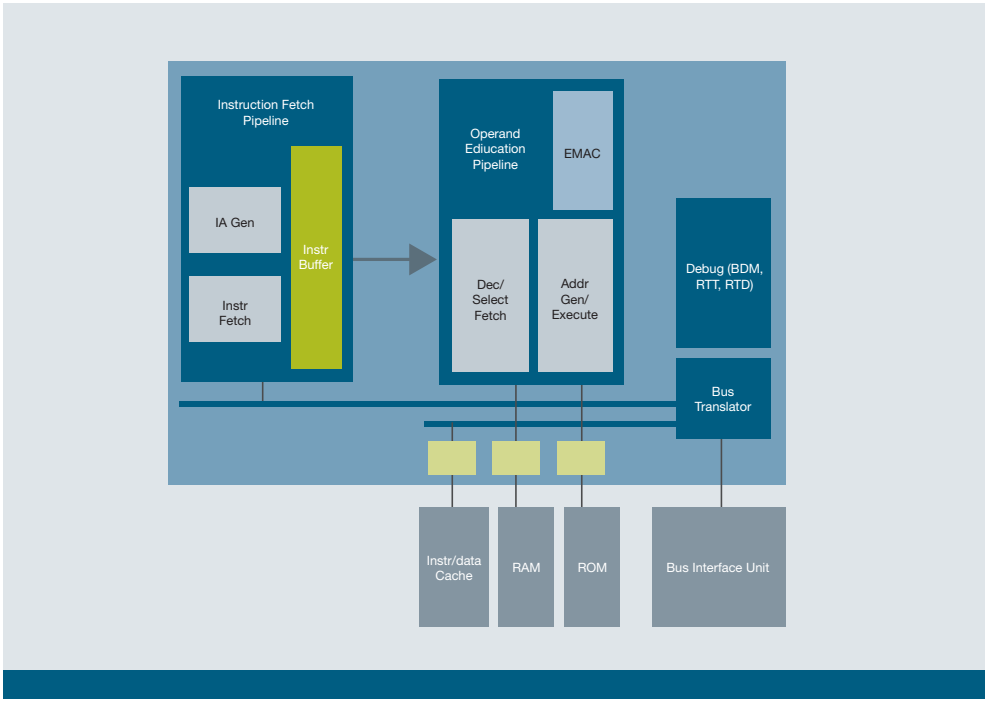
Overview

Freescale Semiconductor proudly introduces an addition to the 68K/ColdFire family of embedded controllers, the intellectual property (IP) for the 68K/ColdFire V2 core architecture for use in application-specific integrated circuit (ASIC) design. The availability of the 68K/ColdFire V2 core architecture for license enables high-volume manufacturers to create their own low-power, highly integrable, 32-bit ASIC solutions that contain a core processor and their own proprietary technology.

The 68K/ColdFire V2 core is based on a memory-configurable hierarchical architecture that is 100 percent synthesizable and specifically designed for reuse and ease of integration into custom designs. The core supports up to 166 MHz of performance on a 0.13 um process using a single-issue, standard cell-based design with 32-bit address and data buses and an integrated debug module. The core uses a variable length RISC architecture that allows instructions to be 16, 32, or 48 bits in length. The result is more efficiently packed code in memory, reducing memory requirements and lowering overall system cost.

ASIC designs based on the V2 core will be software compatible with all ColdFire standard products and cycle accurate with V2-based devices.

V2 Core Block Diagram



Architectural Features

- Variable-length RISC, clock multiplied core
- Independent, decoupled pipelines
  - Two-stage instruction fetch pipeline (IFP)
  - Two-stage operand execution pipeline (OEP)
  - FIFO instruction buffer is the decoupling mechanism
- 16 user-accessible, 32-bit wide general purpose registers
- 32-bit data bus
- 32-bit address bus supporting a 4 Gigabyte linear addressing range
- Sophisticated two-level branch acceleration mechanisms minimize change-of-flow execution time
- Background debug module (BDM), real-time trace (RTT) and real-time debug (RTD) support
- Binary object code compatibility across the entire 68K/ColdFire family
- Enhanced multiply-accumulate (EMAC) execute engine provides high-speed signal processing capabilities with four 40-bit accumulators and single-cycle instruction issue rate on 32 x 32 +_ 32 MAC operations
- Vector base register to relocate the exception-vector table
- 100 percent synthesizable and technology-independent designs

Implementation

- Fully synthesizable, retargetable core
- 166 MHz, 160 Dhry 2.1 MIPS (0.13 um)
- ~50k gates for V2 core only

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Applications

ASICs containing the 68K/ColdFire V2 core architecture deliver control, connectivity and security to a growing number of industrial and commercial applications. ColdFire standard products can be found in health care instrumentation, point-of-sale terminals, factory automation and fire and security systems, as well as in many other industrial and consumer applications. Fast product cycle times and low system costs help give you a competitive edge.

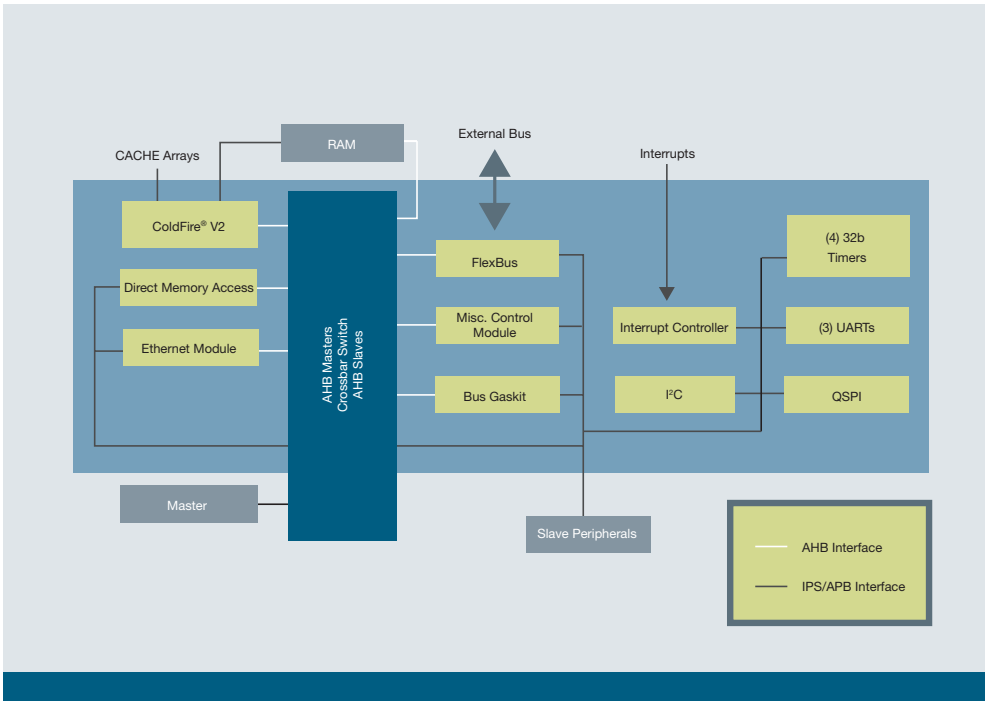
Tools and Support

The entire 68K/ColdFire family of embedded controllers, including the 68K/ColdFire V2 core architecture, is supported by world-class development tools suites offered through leading third-party tools developers. The CodeWarrior® Special Edition software suite for ColdFire is the recommended option, but professional tools from Freescale partners, such as Green Hills, Wind River Systems, Accelerated Technology, ARC and others are available.

Availability

The V2 ColdFire® core and standard product platform (SPP) is now available for licensing through semiconductor IP licensing specialists, IPextreme Inc. Specifically, IPextreme will market, license and support the V2 ColdFire core to System-on-Chip (SoC) designers seeking to integrate the core and other functions onto a single chip, helping them save time and money. Freescale plans to open licensing to additional ColdFire cores in 2007 and beyond. For more information about the ColdFire architecture licensing program or to obtain a license to the V2 ColdFire from IPextreme, visit **www.ip-extreme.com/IP/coldfire_v2.html**.

SPP Block Diagram



Standard Product Platform (SPP)

To help designers decrease time to market, Freescale has packaged the 68K/ColdFire V2 core architecture into a standard product platform. The SPP is a set of tested and previously deployed subsystems and peripherals easily used to build large, complex systems.

SPP Features

- V2 ColdFire core—100–160 MHz
- EMAC module, HW divide
- AXBS (multi AHB crossbar switch) connects multiple masters with various slave IP blocks
- External bus interface (16- or 32-bit)
- DFT emphasis for SoC functional fault coverage and test
- Muxed DFF rising-edge clocked design
- Static timing analysis
- Range of cache and local memory sizes, pipeline options
- Integrated peripherals
  - 10/100 Fast Ethernet controller with DMA
  - QSPI
  - I²C
  - Three UARTs
  - DMA
  - Chip selects, general-purpose I/Os
  - Four 32-bit timers
  - World-class background debug module

Learn More: For more information about ColdFire family products, please visit **www.freescale.com/coldfire**.

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