ColdFire® Embedded Controllers
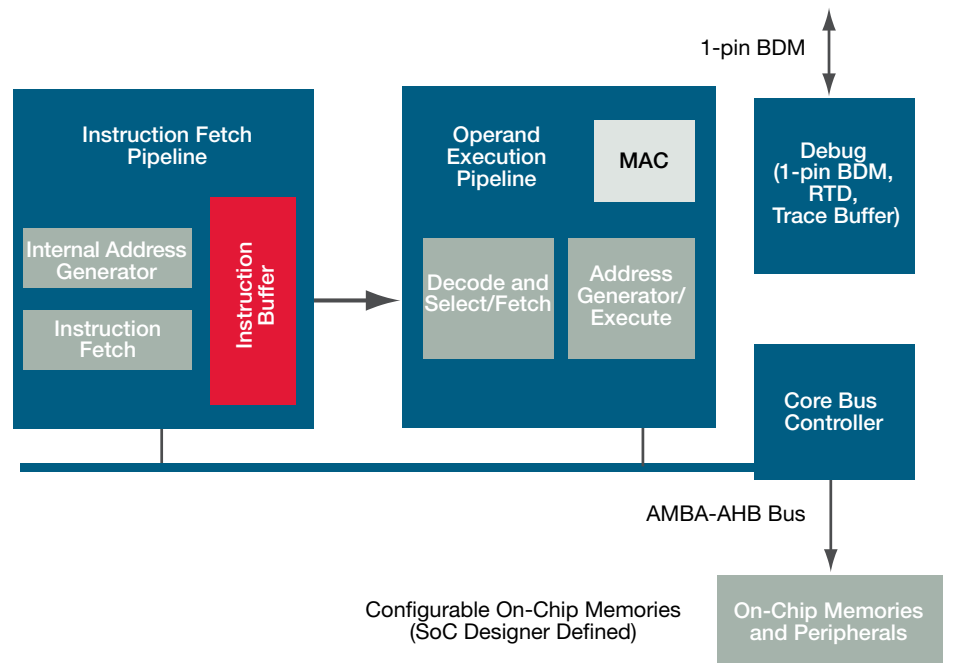
V1 ColdFire® Core Architecture

Target Applications
- Consumer electronics
- Handheld and remote terminals
- Health care instruments and monitoring equipment
- Factory automation systems
- Building monitor and control systems
- Security/access systems
- Office/home automation

Overview

The V1 ColdFire core is a simplified version of the V2 ColdFire core, featuring the same address modes and instruction definitions. It is a memory-configurable hierarchical architecture that is 100 percent synthesizable, specifically designed for reuse and ease of integration into custom designs. The 32-bit core supports up to 150 MHz performance using a standard cell-based design methodology in a generic 130 nm process technology and interfaces to the System-on-Chip (SoC) using the standard AMBA-AHB bus. The core supports a variable-length RISC architecture that allows instructions to be 16, 32 or 48 bits in length. The result is more efficiently packed code in memory, reducing memory requirements and lowering overall system cost.

V1 ColdFire® Core Block Diagram

Instruction Fetch Pipeline
- Internal Address Generator
- Instruction Fetch
- Instruction Buffer

Operand Execution Pipeline
- MAC
- Decode and Select/Fetch
- Address Generator/Execute

1-pin BDM

Debug (1-pin BDM, RTD, Trace Buffer)

Core Bus Controller

AMBA-AHB Bus

Configurable On-Chip Memories (SoC Designer Defined)

On-Chip Memories and Peripherals

The V1 ColdFire core features a single-wire background debug interface with on-chip in-circuit emulator (ICE) debug module. The core also implements a processor status trace buffer to support real-time trace capabilities mapped into a background debug module (BDM) readable resource.

All ColdFire cores (V1, V2, V3 and V4) share the same architecture and instruction set. They are downward and upward code compatible, so drivers will require minimal rewrite.

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Architectural Features

- Variable length RISC
  - 16-bit, 32-bit, and 48-bit instructions
- 16 user-accessible, 32-bit wide general purpose registers
- 32-bit data bus with 24-bit address bus supporting 16 MB linear addressing
- 1-pin BDM, real-time debug (RTD) and on-chip trace buffer support
- Independent, decoupled pipelines
  - 2-stage instruction fetch pipeline (IFP)
  - 2-stage operand execution pipeline (OEP)
  - FIFO instruction buffer provides decoupling
- Multiply accumulate (MAC) provides DSP capabilities
- Standard AMBA-AHB 2.0 Interface
  - 2-stage pipelined bus, 32-bit implementation

Implementation

- Fully synthesizable, retargetable core
- 150 MHz, 158 Dhry 2.1 MIPS (130 nm)
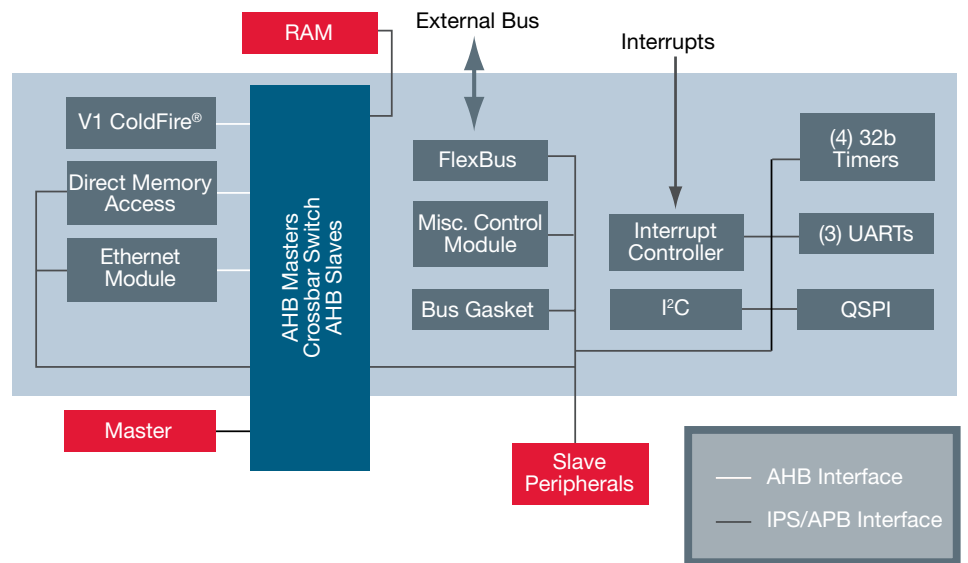- ~43 Kgates for V1 core only

Standard Product Platform–SPP

To help designers decrease time to market, Freescale has packaged the V1 ColdFire core architecture into a standard product platform (SPP). The SPP is a set of tested and previously deployed subsystems and peripherals easily used to build large complex systems. It has been designed to share the same peripheral set included on many ColdFire standard devices, leveraging the extensive peripheral portfolio to enhance end-use applications with the latest features and capabilities.

Features:

- V1 ColdFire core—Up to 150 MHz in 130 nm process technology
- MAC module, HW divide
- External bus interface (16- or 32-bit)
- DFT emphasis for SoC functional fault coverage and test
- Muxed DFF rising-edge clocked design
- Static timing analysis

SPP Block Diagram

- Single-pin BDM interface
- Integrated peripherals
  - 16-channel direct memory access (DMA)
  - Fast Ethernet controller
  - Multi-master crossbar switch
  - FlexBus for external interface
  - Interrupt controller
  - Four 32-bit DMA timers
  - Three universal asynchronous receiver and transmitters (UARTs)
  - Queued serial peripheral interface (SPI)
  - I²C
  - On-platform peripheral expansion bus

Tools and Support

The entire ColdFire core architecture is supported by world-class development tool suites offered through leading third-party tools developers. CodeWarrior® Special Edition software suite for ColdFire is the recommended option, but professional tools from Freescale partners, such as Green Hills, Wind River Systems, Accelerated Technology, ARC and others are available.

Availability

The V1 ColdFire core is available now for licensing through IPextreme Inc., a value-added reseller and technology support center for semiconductor IP. Specifically, IPextreme markets, licenses and supports the V1 ColdFire core to SoC designers seeking to integrate the core and other functions onto a single chip, helping them create customized solutions saving time and money.

For more information about the ColdFire architecture licensing program or to obtain a license to the V1 ColdFire core from IPexteme, visit **www.ip-extreme.com**.

Learn More: For more information about ColdFire family products, please visit **www.freescale.com/coldfire.**