Fact Sheet

M-2 UTOPIA / POS-PHY ADAPTER REFERENCE DESIGN

PRELIMINARY

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FEATURES

- *Adapts the C-3e and C-5e Network Processor interfaces to support single-PHY and multi-PHY Utopia and POS-PHY L2, 16 bit interfaces*
- *Connects to either a Channel Processor cluster interface or the Fabric Processor Utopia-like interface*
- *Provides up to OC-12 full-duplex bandwidth*
- *Supports up to 16 addressable devices*
- *Supports frame sizes from 5 to 65535 bytes in 64 byte chucks on POS-PHY*
- *Supports 54-byte ATM cells, on 16-bit UL-2 interface, and 52-byte ATM cells plus up to 12 cell tags on the C-3e/C-5e NP interface*
- *Offers lower total system cost*

Motorola's M-2 Utopia/POS-PHY Adapter Reference Design is designed to seamlessly connect the C-Port family of network processors (NPs) to the ever-growing list of Utopia Level-2 (UL-2) and POS-PHY Level-2 (PL-2) physical inter-face chips, supporting both SPHY and MPHY implementations. Typical applications for the M-2 adapter include DSLAMs, ATM aggregation devices, multiservice platforms, wireless infrastructure devices, and media gateways.

The M-2 adapter will be provided as a complete reference design to customers, including the source RTL code, fitted binary files and, NP application code. This turnkey solution delivers a very low-cost, small-footprint device using the supplied reference software, and simplifies the design of systems needing Utopia/POS-PHY functionality. Additionally, the M-2 adapter can be matched to a range of applications by tailoring the source code.

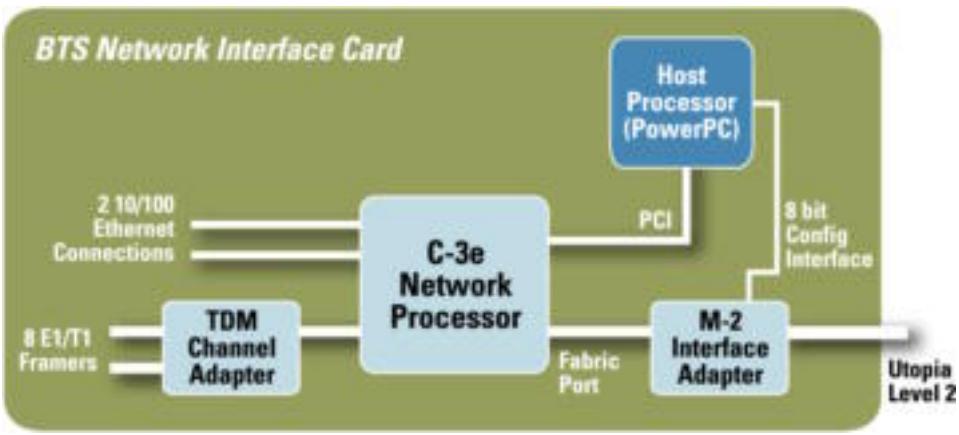
Current C-Port family NPs support single-channel physical interface (SPHY) devices, as defined under Utopia Level-2/3 (UL-2/UL-3), that can be connected to the NP's Fabric Processor (FP). The M-2 adapter allows 16 UL-2 or PL-2 PHY devices to be connected to the C-3e/C-5e NP's Channel Processor (CP) cluster and 16 UL-2 PHY devices to be connected to the FP. The M-2 adapter's multiple configurations allow connection to a wide variety of UL-2 and PL-2 framers supporting an aggregate bit rate of 622Mb. The maximum clock rate for the M-2 adapter is 50 Mhz.

UL-2/PL-2 FRAMER INTERFACE

The UL-2/PL-2 connection is designed to connect to ATM PHY devices that implement the UL-2 or PL-2 with 16 bit interfaces. Parity is also supported and is globally selected. The MPHY addresses to be polled are set by the source code. To reduce cost in the FPGA, PL-2 is only supported on the CP cluster connection.

The M-2 adapter supports cell sizes of 54 bytes for 16-bit interfaces. Active MPHY addresses are set via the configuration registers.

Frame sizes can be from 5 to 65,535 bytes. The maximum data chunk size passed to the C-5e/C-3e NP is 64 bytes per MPHY address. The final chunk can be up to 127 bytes to efficiently support data streams where packet sizes are greater than 64 bytes. Only packet mode polling is supported. Active MPHY addresses are set via the configuration registers.



Wireless basestation (BTS) line card diagram including the M-2 Utopia / POS-PHY Adapter connected to the C-3e Network Processor

For More Information On This Product,
Go to: www.freescale.com

PRODUCT PACKAGING

The product packaging includes:

- Verilog RTL (fully commented)
- Fitted binary code
- Target FPGA part number and pinout
- CP or FP microcode
- Application notes and full documentation

Several configurations will be available.

NPU Connection	Configuration	Device
Channel Processors	UL2-SPHY	FPGA
	PL2-SPHY	FPGA
	UL2-MPHY	FPGA
	PL2-MPHY	FPGA
Fabric Processor	UL2-MPHY	FPGA

To increase flexibility, reduce cost, and meet the needs of a range of applications, different size FPGAs, supporting 4, 8, or 28 MPHYs can be implemented based on application requirements.

SOFTWARE SUPPORT

The C-Ware Software Toolset (CST) will include a set of configuration APIs for the M-2 adapter. The APIs will be provided in source code and will support the development of drivers that control and configure the M-2 adapter in target systems. You will be able to easily modify the source code and add features as needed by your design.The CST will also support the modeling of input and output data via traffic generators that mimic the M-2 adapter's interface to the C-3e/C-5e NP.

HARDWARE SUPPORT

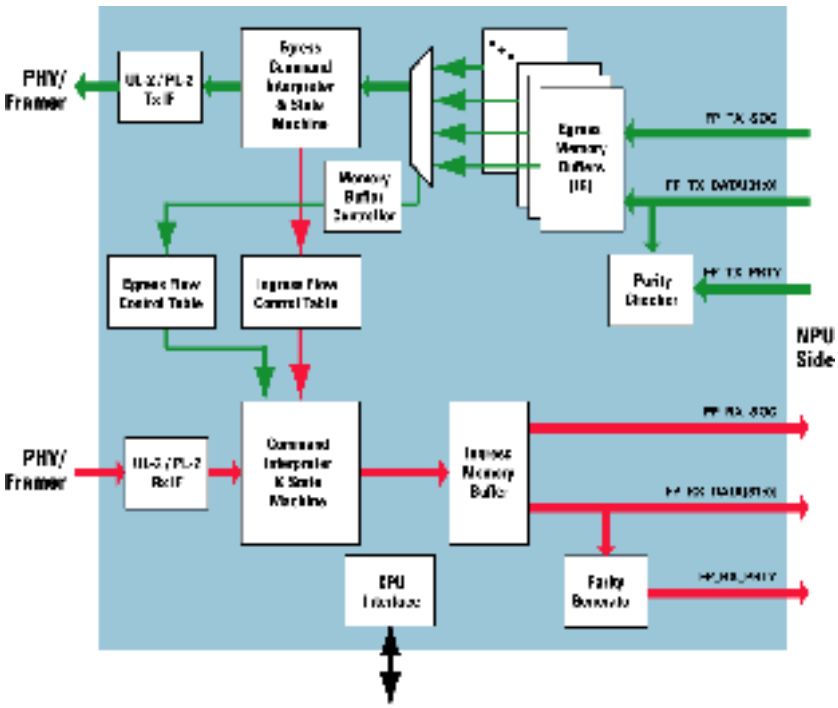
A C-Ware Development System (CDS) Physical Interface Module (PIM) supporting the M-2 adapter will be available. The PIM will support, at up to OC-12 data rates, PL-2/UL-2 to a CP cluster and UL-2 out of the FP.

NETWORK PROCESSOR (NPU) INTERFACE

The NPU side of the M-2 adapter is designed to connect to either a CP cluster or to the FP on a C-3e/C-5e NP. When connected to the CP cluster, the interface is a modified GMII interface. When connected to the FP, the interface is similar to 16 bit Utopia UL-2, but it is not a full implementation of the standard. The FP uses an in-band flow-control mechanism.

HOST PROCESSOR (CPU) INTERFACE

Configuration parameters can either be set as defaults in the RTL code or can be programmed into the M-2 adapter via its CPU interface. The interface is an 8 bit parallel asynchronous interface.



Block Diagram of the M-2 Utopia / POS-PHY Adapter

For more information about Motorola's network processing solutions, please contact your local Motorola sales representative or call (800) 521-6274. You can also visit Motorola's Smart Networks Web site at:

www.motorola.com/networkprocessors

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