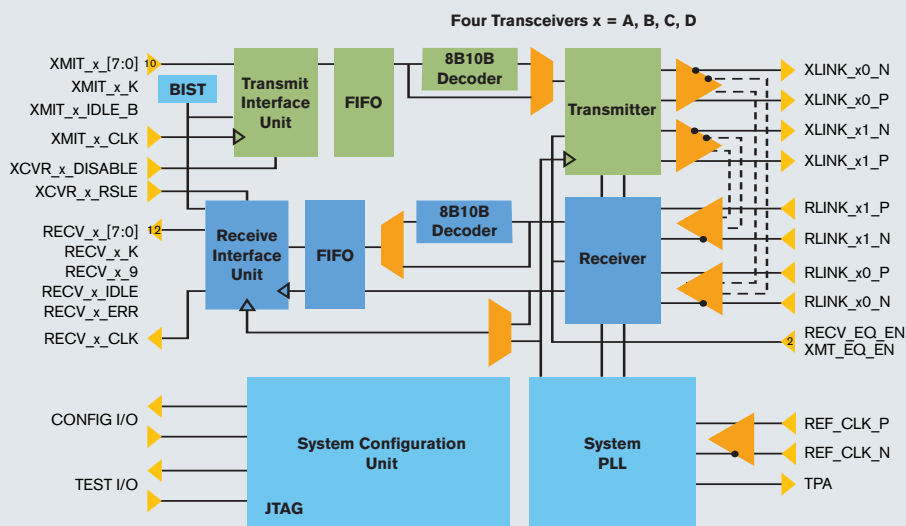


MC92610 QUAD

The MC92610 Quad is a high-speed, full-duplex, serializer/deserializer (SERDES) data interface that can be used to transmit data between chips across a board, through a backplane, or through cabling. Four transceivers transmit and receive coded data at a rate of 2.5 gigabit per second (Gbps) through each 3.125 gigabaud link. A rich feature set makes it easily adaptable to many broadband applications. The MC92610 is the latest generation in Freescale's SERDES product line. Like its predecessors, it features a very low power 0.25 micron CMOS implementation that nominally consumes less than 1800 mW with all links operating at full speed.

MC92610 QUAD SERDES BLOCK DIAGRAM



Product highlights

- > Four full-duplex differential data links
- > 20 Gbps data aggregate transfer speed
- > Dual speed range: 3.125 Gbaud or 1.25 Gbaud
- > Low power: 1800 mW, under typical conditions, with all transceivers operating at full speed
- > Transceiver channels may be individually disabled
- > IEEE Std 1149.1 JTAG support and full-speed built-in self test, BIST, functions

Typical applications

- High-speed data transfer applications in high-bandwidth backplane and chassis-to-chassis networking
- > High-end router systems
- > Backbone switches
- > Access switches
- > Storage Area Network equipment
- > High-speed Automatic Test Equipment

Data interface

- > Internal Fibre Channel 8B/10B encoder/decoder accessed through Byte Interface or bypassed in Ten-Bit Interface mode
- > Double DataRate (DDR), source synchronous, 8-bit and 10-bit HSTL parallel data interfaces
- > Link Multiplex Mode enables operation of two links with Single Data Rate (SDR), source synchronous, 16-bit and 20-bit parallel data interfaces
- > Selectable Idle character alignment mode enables transfers with automatic realignment or unaligned data transfers
- > Link-to-link synchronization supports aligned, 32-bit, word transfers. Synchronization mechanism tolerates up to 40-bit times of link-to-link media delay skew
- > Multi-chip link synchronization supports aligned multi-word transfers. Up to four devices may be combined to provide 128-bit, four-word, synchronized transfers

- > Each channel has dedicated input clock (≥ 156.25 MHz)
- > Received data may be clocked at the recovered clock or the reference clock frequency

Link interface

- > Links drive 50-ohm media (100-ohm differential), backplane or cable
 - On-chip link termination (no external terminating resistors needed)
 - On-chip coupling capacitors provide expanded input common mode range
- > Link inputs are "hot-swap" compatible
- > Selectable transmit and receive equalization
- > Repeater mode configures the device into a four-link receive-transmit repeater
- > Redundant transmitter link outputs and receiver link inputs
- > Redundant links are selectable per transceiver
- > Broadcast mode enables all transmit links

Parametrics

- > Power Supply
 - Core Power Supply: $1.8\text{ V} \pm 0.15\text{ Vdc}$
 - HSTL I/O Power Supply: $1.5\text{ V} \pm 0.10\text{ Vdc}$ or $1.8\text{ V} \pm 0.15\text{ Vdc}$
 - Link I/O Power Supply: $1.8\text{ V} \pm 0.15\text{ Vdc}$
- > Power Dissipation Typical operation: $<450\text{ mW}$ per channel at maximum speed

Package

- > 324 pin MAPBGA (19x19 mm body size, 1.0 mm ball pitch)

Technical specifications

- > All channels have:
 - 8B/10B encoder/decoder that can be enabled or bypassed
 - Clock generation/recovery
 - Idle/control character generation/detection
 - Independent 8-bit or 10-bit system I/F with parallel-to-serial, serial-to-parallel conversion
- > Transceiver Links operate over 50-ohm media (100-ohm differential) for lengths of up to 1 meter of FR-4 board/back-plane, or six meters of coax
- > No external loop filter or termination components required
- > In-system BIST test modes
- > At speed, in circuit, with error counter
- > In-system loopback BIST isolated from link inputs and outputs
- > IEEE Std 1149.1 JTAG boundary scan support
- > Differential reference clock input with single-ended reference clock input option (156.25 MHz max)
- > Tolerates REF_CLK frequency offset in excess of ± 200 ppm
- > Technology: High-performance 0.25 μ CMOS Process, five-layer metal

Learn More: For more information about Freescale products, visit www.motorola.com/semiconductors