Fact Sheet

MPC107

PCI BRIDGE MEMORY CONTROLLER

The MPC107 PCI Bridge/Integrated Memory Controller provides a bridge between the Peripheral Component Interconnect (PCI) bus and Motorola MPC6xx, MPC7xx, and MPC74xx microprocessors. PCI support allows system designers to design systems quickly using peripherals already designed for PCI and the other standard interfaces available in the personal computer hardware environment. The MPC107 provides many of the other necessities for embedded applications, including a high-performance memory controller and dual-processor support; two-channel flexible DMA controller; an interrupt controller; an I_2O-ready message unit; an inter-integrated circuit controller (I^2C); and low-skew clock drivers. The MPC107 contains an Embedded Programmable Interrupt Controller (EPIC) featuring five hardware interrupts (IRQs) as well as 16 serial interrupts along with four timers. The MPC107 uses an advanced, 2.5V HiP3 process technology and is fully compatible with TTL devices.

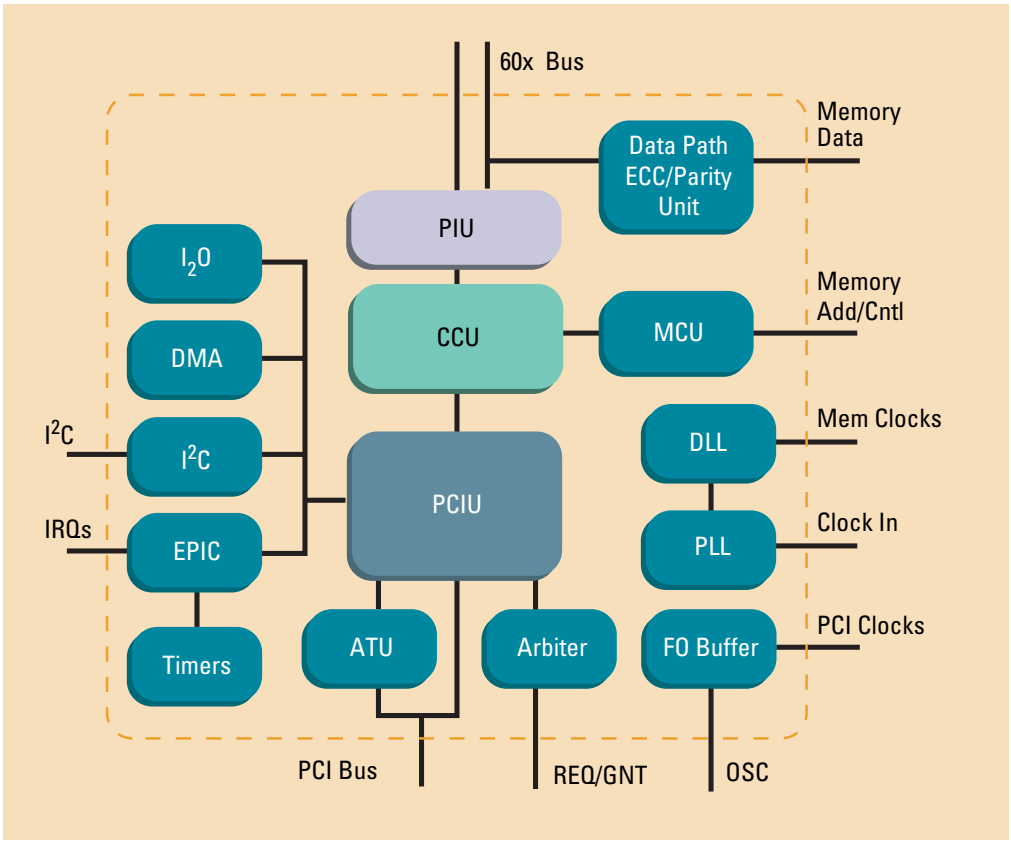
INTEGRATED MEMORY CONTROLLER

The memory interface controls processor and PCI interactions to main memory. It supports a variety of programmable timing supporting DRAM (FPM, EDO), SDRAM, and ROM/Flash ROM configurations, up to speeds of 100 MHz.

PCI BUS SUPPORT

The MPC107 PCI interface is designed to connect the processor and memory buses to the PCI local bus without the need for "glue" logic at speeds up to 66 MHz. The MPC107 acts as either a master or slave device on the

MOTOROLA MPC107 BLOCK DIAGRAM



PCI bus and contains a PCI bus arbitration unit which reduces the need for an equivalent external unit, thus reducing the total system complexity and cost.

MULTIPROCESSOR AND LOCAL BUS SLAVE SUPPORT

The MPC107 supports a programmable interface to microprocessors implementing the PowerPC architecture operating at bus frequencies up to 100 MHz. The MPC107 processor interface allows for a variety of system configurations by providing support for a second processor and a local bus slave.

MPC107 MAJOR FEATURES

Memory Interface

- High-bandwidth (32-bit/64-bit) data bus up to 100 MHz
- Programmable timing supporting either DRAM (FPM, EDO) or SDRAM
- Supports one to eight banks – 4-, 16-, 64-, 128-, and/or 256-bit DRAMs or SDRAMs
- 1 GB of RAM space, 144 MB of ROM space
- 8-, 32-, or 64-bit ROM/Flash ROM
- PortX: 8-, 32-, or 64-bit general-purpose I/O port uses ROM controller interface with address strobe
- Supports parity, read-modify-write, or error-correcting code (ECC)

Processor Interface

- Processor bus frequency up to 100 MHz
- 64-bit or 32-bit data bus and 32-bit address bus
- SMP support for a second processor
- Full memory coherency supported, integrated arbiter, and slave peripheral support
- Supports MPC6xx, MPC7xx, and MPC74xx processors

PCI Interface

- Compliant with PCI specification, revision 2.1
- 32-bit PCI interface operates up to 66 MHz
- 5.0V compatible
- Read and write buffers to improve PCI performance
- Selectable big- or little-endian operation
- PCI interface can be configured as host or agent, allowing multiple MPC107 chips on same PCI bus
- Arbiter supports up to five other PCI devices
- Parity support

Other Embedded Features

- Two-channel integrated DMA controller
  - Supports direct or chaining modes
  - Scatter gather
  - Interrupt on completed segment, chain, and error
  - Local to local memory
  - PCI to PCI memory
  - PCI to local memory
  - Local to PCI memory
- Message Unit
  - Intelligent Input/Output (I_2O) Message Controller
  - Two door-bell registers
  - Inbound and outbound messaging registers
- Inter-Integrated Circuit (I^2C) Controller
  - Full master/slave support
- Embedded programmable interrupt controller (EPIC)
  - Five hardware interrupts (IRQs) or 16 serial interrupts
  - Four programmable timers
- Integrated PCI bus and SDRAM clock generation
- Programmable memory and PCI bus drivers
- Debug Features
  - Watchpoint monitor
  - Memory attribute and PCI attribute signals
  - JTAG/COP – Common On-board Processor for in-circuit hardware debugging
  - IEEE 1149.1-compliant, JTAG boundary-scan interface
- 503-pin ball grid array (BGA) package

Power Management

- Four levels of power reduction–doze, nap, sleep, and suspend
- Fully static, internal logic states preserved during all power modes

CONTACT INFORMATION

For more information on Motorola processors, point your Web browser to: http://motorola.com/smartnetworks

For all other inquiries about Motorola products, please contact the Motorola Customer Response Center at:
Phone: 800-521-6274 or
http://www.motorola.com/semiconductors

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