

Target Applications

- Electric power steering
- Short- and mid-range adaptive cruise control (up to 100m), RADAR and LIDAR
- Vehicle dynamic and chassis control
- ABS braking systems
- Electronic stability program (ESP)
- Blind spot detection
- Pre-crash detection
- Hybrid electric vehicles

Overview

The Qorivva MPC564xL family of MCUs is part of the SafeAssure program and is designed to specifically address the required IEC61508 (SIL3) and ISO26262 (ASILD) safety standards. It reduces design complexity and component count by putting key functional safety features on a single chip with a dual-core, dual-issue architecture.

In lockstep mode it provides an environment for redundant processing and calculations. Common cause failure countermeasures targeting power, clock and error propagation are implemented to detect various failure modes.

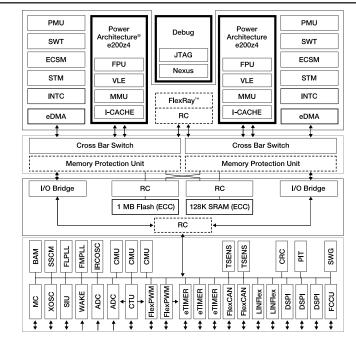


32-bit Power Architecture® MCUs

MPC564xL Family

Safety with flexibility

MPC564xL Block Diagram



The MPC564xL's dual-core, dual-issue architecture can be statically switched from lockstep mode to decoupled parallel mode (independent core operation) for those applications needing maximum performance or software diversity. With dual-issue technology, the cores can process two instructions per clock cycle, enabling more performance and using less power. The MPC564xL family is specifically designed to support actuator control applications for vehicle electrification. Enabled by the new cross-triggering unit, the device allows control of up to two brushless DC motors or multiple valves with only minimum interrupt load. Additional features include the fault collection unit, FlexRay[™] protocol, two 12-bit ADCs, eTimer units and a built-in hardware self test.



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SafeAssure Program:		System Challenges	MPC564xL Solution
Functional Safety. Simplified		Reduce system costs and simplify design	Reduces design complexity and component count by putting key
The Freescale SafeAssure functional			functional safety features on a single chip
safety program is designed to help system			 Dual processing spheres, including CPU, DMA, interrupt controller, crossbar and MPU for logic level fault detection
manufacturers more easily achieve system			Dual z4 CPU architecture provides performance to address real-time
compliance with functional safety standards: International Standards Organization (ISO)			applications and cross-checking functions common in many safety strategies, which reduces hardware and software complexity used in
26262 and 61508. The program highlights			multiple MCU designs. The architecture can be run in two statically
Freescale solutions—hardware and software—			 configurable modes of operation Lockstep operation provides a software environment for redundant
that are optimally designed to support			processing and calculations
functional safety implementations and			 Independent core operation (dual parallel mode) provides a software
come with a rich set of enablement collateral.			environment for diverse processing and calculations to increase performance or to cross check for reliable operation
For more information, visit			Built-in flexible hardware self-test capabilities provide diagnostic
freescale.com/SafeAssure.			coverage both at logic and memory level
Development Tools Compilers			 Fault collection and control unit manages MCU behavior in the event of internal MCU logic faults and signals these to external system components
-			FlexRay protocol and safety ports for robust communications
 Freescale CodeWarrior IDE, visit freescale.com/CodeWarrior for 			 Probability of undetected failure per hour (PFH) = 0.1 FIT
more information			(one failure per every 10 billion hours)Designed to address safety requirements outlined in IEC61508 and
Green Hills			ISO26262, which reduces system cost and effort
Wind River Diab		Precise and	• e200 dual-issue z4 CPU at 120 MHz provides computational
		deterministic control timing for real-time applications, such as motor control	 performance targeted at vector-oriented control of motor applications Dual-core architecture provides computation ability for complex
Debuggers			applications or cross-checking requirements of safety applications
P&E Micro			Precise control of integrated electric motor control periphery
Lauterbach			 Advanced PWM for specialized multi-phase motor control requirements
Green Hills			 Configurable alignment
Runtime Software			 High frequency above 100 MHz
Flash and FEE drivers			 Dead time insertion Skew correction
Software Core Self Test			 Skew correction Cross-triggering unit coordinates ADC, timer and PWM generation
AUTOSAR MCU			and minimizes CPU interrupt load
Abstraction Layer			 eTimer units handle rotor position and speed acquisition and offer six dual-action IC/OC channels with incremental/quadrature encoder
AUTOSAR OS Package Options			mode
			 Two 12-bit ADCs offer precise conversion for improved driving experience
			 FlexRay protocol for fault tolerant communications with other networked modules within the vehicle
Temp Ranges (Ta) Package			Up to 1 MB flash
-40°C to +125°C	144 LQFP		Up to 128K SRAM
			 Motor control library of common functions Ability to control two 2 phase maters ideal for cleatrical steering
			 Ability to control two 3-phase motors, ideal for electrical steering applications
		Low-cost package is	QFP package option
		easy to solder	• Cost effective
		and inspect	Low power Surgeonal loads
			 Exposed leads

Learn more at freescale.com/Qorivva

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