Fact Sheet

MPC7441

HIGH PERFORMANCE, LOW-POWER HOST MICROPROCESSOR

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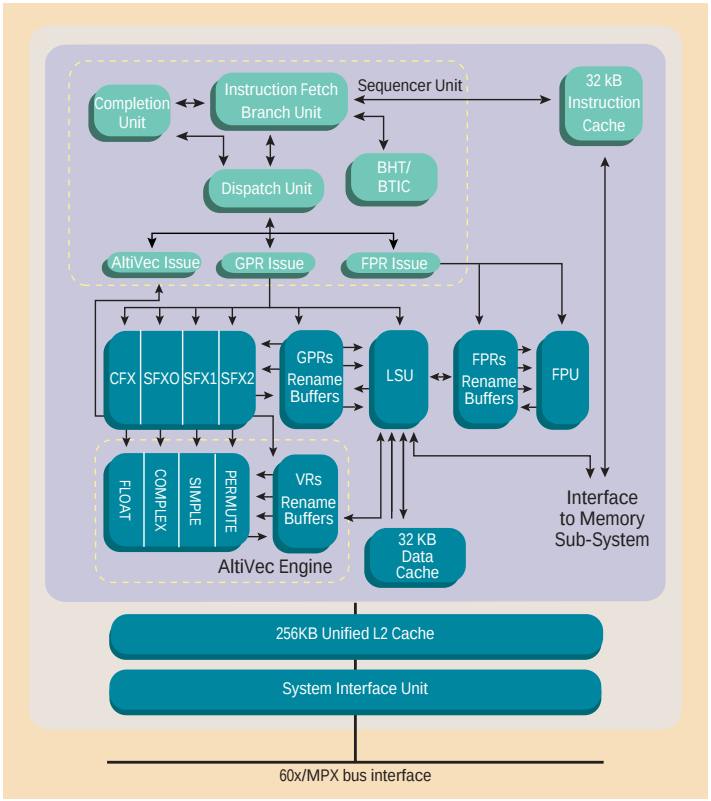
The MPC7441 microprocessor is a high-performance, low-power, 32-bit implementation of the PowerPC RISC architecture with a full 128-bit implementation of Motorola's AltiVec™ technology. This microprocessor is ideal for leading-edge computing, embedded network control, and signal processing applications. The MPC7441 has a deep, seven-stage pipeline with 11 execution units. The L2 cache has been integrated onto the die for greater speed, and a 256-bit datapath to the L1 cache has been implemented. The MPC7441 offers increased address space and high-bandwidth MPX bus with minimized signal setup times and reduced idle cycles to increase bus bandwidth to a maximum speed of 133 MHz MPC7441 processors offer single-cycle, throughput, double-precision, floating-point performance and full symmetric multiprocessing (SMP) capabilities. Finally, the MPC7441 is software-compatible with existing MPC6xx, MPC7xx, and MPC74xx processors and exploits the full potential of AltiVec technology.

SUPERSCALAR MICROPROCESSOR

MPC7441 microprocessors feature a high-frequency, superscalar PowerPC core, capable of issuing four instructions per clock cycle (three instructions + branch) into 11 independent execution units:

- Four integer units (3 simple + 1 complex)
- Double-precision floating-point unit
- Four AltiVec units (simple, complex, floating, and permute)
- Load/store unit
- Branch processing unit

MOTOROLA MPC7441 BLOCK DIAGRAM



CACHE AND MMU SUPPORT

The MPC7441 microprocessor has separate 32 KB, physically addressed instruction and data caches. Both L1 caches feature cache way locking and are eight-way set associative. This L2 is 256 KB eight-way set associative. L2 cache access is fully pipelined. Finally, in addition to supporting hardware table searching, the MPC7441 can be configured for software table searching. In this case, TLB entries are loaded by the system software.

The MPC7441 microprocessor contains separate memory management units for instructions and data, supporting 4 petabytes (2^{52}) of virtual memory and up to 64 GB (2^{36}) of physical memory. The MPC7441 also has four instruction block address translation and four data block address translation registers.

MPX BUS INTERFACE

MPC7441 microprocessors support the MPX bus protocol with a 64-bit data bus and a 32- or 36-bit address bus. Support is included for burst, split, pipelined, and out-of-order transactions, in addition to data streaming and data intervention (in SMP systems). The interface provides snooping for data cache coherency. The MPC7441 implements the cache coherency protocol for multiprocessing support in hardware, allowing access to system memory for additional caching bus masters, such as DMA devices.

POWER MANAGEMENT

MPC7441 microprocessors feature a low-power 1.5V design with three power-saving user-programmable modes—nap, doze (with bus snoop), and sleep—which progressively reduce the power drawn by the processor.

ALTIVEC TECHNOLOGY

AltiVec technology expands the capabilities of Motorola's fourth generation of microprocessors implementing the PowerPC architecture by providing leading-edge, general-purpose processing performance while concurrently addressing high-bandwidth data processing and algorithmic-intensive computations in a single-chip solution.

ALTIVEC TECHNOLOGY:

- Meets the computational demands of networking infrastructure, such as echo cancellation equipment and basestation processing.
- Enables faster, more secure encryption methods optimized for the SIMD processing model.
- Provides compelling performance for multimedia-oriented desktop computers, desktop publishing, and digital video processing.
- Enables real-time processing of the most demanding data streams (MPEG-2 encode, continuous speech recognition, real-time high-resolution 3-D memory for 3-D graphics.)

CONTACT INFORMATION

Motorola offers user's manuals, application notes, sample code, and full local support for all of its processors. For more information, visit: http://motorola.com/smartnetworks

For all other inquiries about Motorola products, please contact the Motorola Customer Response Center at: 1-800-521-6274 or http://motorola.com/semiconductors

MPC7441 Host Processor	
CPU Speeds – Internal	600 and 700 MHz
Bus Frequency	133 MHz
Bus Interface	64-bit
Bus Protocol	MPX/60x
Instructions per Clock	4 (3 + Branch)
Integrated L1 Cache	32 KB instruction 32 KB data
Integrated L2 Cache	256 KB
Typical/Maximum Power Dissipation	11.4/15.4W @ 600 MHz 13.4/17.9W @ 700 MHz
Package	360 CBGA
Process	0.18µ 6LM CMOS
Voltage	1.5V internal, 1.8/2.5V I/O
Other Performance	Drystone 2.1: 1083 MIPS @ 600 MHz 1264 MIPS@ 700 MHz
Execution Units	Integer(4), Floating-Point, AltiVec(4), Branch, Load/Store

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