

MPC7450/MPC7451

High Performance Host Microprocessor

The MPC7450/MPC7451 host processor is a high-performance, low-power, 32-bit implementation of the PowerPC RISC architecture with a full 128-bit implementation of Motorola's AltiVec technology. This microprocessor is ideal for leading-edge computing, embedded network control, and signal processing applications. The MPC7450/MPC7451 has a deep, seven-stage pipeline with 11 execution units. The L2 cache has been integrated onto the die for greater speed, and supports a large backside L3 cache with a 64-bit datapath. The MPC7450/MPC7451 offers increased address space and high-bandwidth MPX bus with minimized signal setup times and reduced idle cycles to increase bus bandwidth to a maximum speed of 133 MHz. MPC7450/MPC7451 processors offer single-cycle throughput double precision floating-point performance and full sym-

metric multi-processing (SMP) capabilities. Finally, the MPC7450/MPC7451 is software-compatible with existing MPC6xx, MPC7xx, and MPC74xx host processors and exploits the full potential of AltiVec technology.

Superscalar Microprocessor

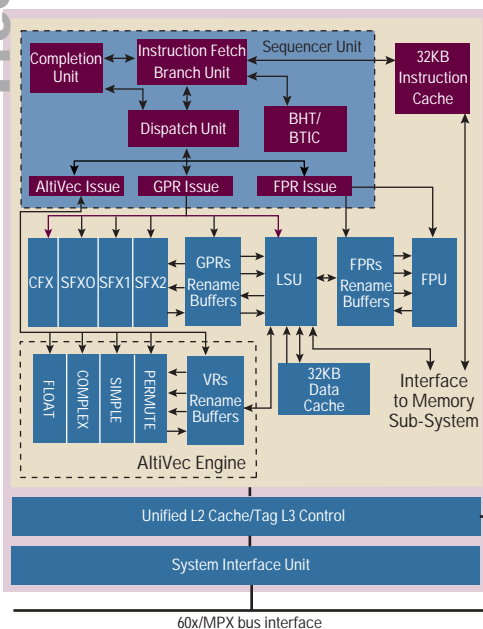
MPC7450/MPC7451 microprocessors feature a high-frequency superscalar G4 core, capable of issuing four instructions per clock cycle (three instructions + branch) into eleven independent execution units:

- Four integer units (3 simple + 1 complex)
- Double-precision floating-point unit
- Four AltiVec units (simple, complex, floating, and permute)
- Load/store unit
- Branch processing unit

Cache and MMU Support

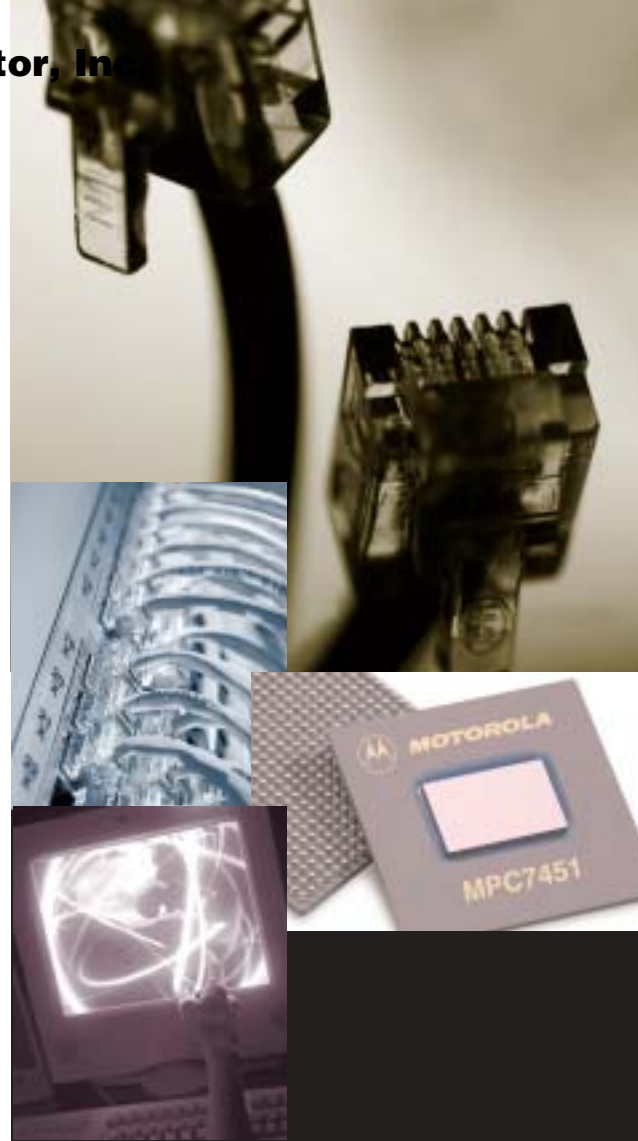
The MPC7450/MPC7451 microprocessor has separate 32KB, physically addressed instruction and data caches. Both L1 caches feature cache way locking and are eight-way set associative. For greater speed, the L2 cache has been integrated on-chip with a 256-bit interface to L1 which operates at processor frequency. This L2 is 256KB eight-way set associative. L2 cache access is fully pipelined. The MPC7450/MPC7451 also supports an L3 cache interface with on-chip tags

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MPC7450/MPC7451 Block Diagram

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	MPC7450/MPC7451
CPU Speeds – Internal	533, 667 and 733, and 867MHz
Bus Frequency	133MHz
Bus Interface	64-bit
Bus Protocol	MPX/60x
Instructions per Clock	4 (3 + Branch)
Integrated L1 Cache	32 KB instruction 32 KB data
Integrated L2 Cache	256 KB
L3 Cache	1 or 2 MB
Typical/Maximum Power Dissipation	14W /17W @ 533MHz
Die Size	106 mm ²
Package	483 CBGA
Process	0.18µ 6LM CMOS
Voltage	1.8V internal, 1.8/2.5V I/O
SPECint95 (estimated)	32.1 @ 733MHz
SPECfp95 (estimated)	23.9 @ 733MHz
Other Performance	1324 Drystone 2.1 MIPS @ 733MHz
Execution Units	Integer(4), Floating-Point, Altivec(4), Branch, Load/Store

Contact Information

Motorola offers user's manuals, application notes, sample code and full local support for all of its processors. For more information, visit: <http://motorola.com/smartnetworks>

For all other inquiries about Motorola products, please contact the Motorola Customer Response Center at: 1-800-521-6274 or <http://motorola.com/semiconductors>

to support up to 2MB of off-chip cache. The L3 data bus is 64-bits wide, provides multiple SRAM options, and affords critical quad-word forwarding to reduce latency. The off-chip L3 storage can also be configured as a local addressable memory. Finally, in addition to supporting hardware table searching on a TLB miss, the MPC7450/MPC7451 can be configured for software table searching. In this case, TLB entries are loaded by the system software.

The MPC7450/MPC7451 microprocessor contains separate memory management units for instructions and data, supporting 4 Petabytes (2⁵²) of virtual memory and up to 64 Gigabytes (2³⁶) of physical memory. The MPC7450/MPC7451 also has four instruction block address translation and four data block address translation registers.

MPX Bus Interface

MPC7450/MPC7451 microprocessors support the MPX bus protocol with a 64-bit data bus and a 32- or 36-bit address bus. Support is included for burst, split, pipelined and out-of-order transactions, in addition to data streaming, and data intervention (in SMP systems). The interface provides snooping for data cache coherency. The MPC7450/MPC7451 implements the cache coherency protocol for multiprocessing support in hardware, allowing access to system memory for additional caching bus masters, such as DMA devices.

Power Management

MPC7450/MPC7451 microprocessors feature a low-power 1.8-volt design with three power-saving user-programmable modes -- nap, doze (with bus snoop) and sleep -- which progressively reduce the power drawn by the processor.

Altivec Technology

The Altivec technology expands the capabilities of Motorola's fourth generation microprocessors by providing leading-edge, general purpose processing performance while concurrently addressing high-bandwidth data processing and algorithmic-intensive computations in a single-chip solution.

Altivec technology:

- Meets the computational demands of networking infrastructure such as echo cancellation equipment, and basestation processing.
- Enables faster, more secure encryption methods optimized for the SIMD processing model.
- Provides compelling performance for multimedia-oriented desktop computers, desktop publishing, and digital video processing.
- Enables real-time processing of the most demanding data streams (MPEG-2 encode, continuous speech recognition, real-time high-resolution 3D memory for 3D graphics.)



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