Integrated Host Processors

MPC8241 Host Processor Built on Power Architecture™ Technology

Overview
The MPC8241 integrated host processor implementing a core based on Power Architecture™ technology fits applications where cost, space, power consumption and performance are critical requirements. This device is designed to provide a high level of integration, reducing chip count from five discrete chips to one, thereby significantly reducing system component cost. High integration results in a simplified board design, low power consumption and a faster time to market solution. This cost-effective, general-purpose integrated processor targets systems using Peripheral Component Interconnect (PCI) interfaces in networking infrastructure, telecommunications and other embedded markets. It can be used for control processing in applications such as routers, switches, network storage applications and image display systems.

Product Highlights
• 166 MHz–266 MHz processor core
• 32-bit PCI interface operating at up to 66 MHz
• Memory controller offering SDRAM support up to 133 MHz operation, support up to 2 GB
• General-purpose I/O and ROM interface support
• Two-channel DMA controller that supports chaining
• Messaging unit with I/O messaging support capability
• Industry-standard I²C interface
• Programmable interrupt controller with multiple timers and counters
• 16550 compatible dual universal asynchronous receiver/transmitter (DUART)

Typical Applications
• Wireless LAN
• Routers/switches
• Embedded computing
• Multi-channel modems
• Network storage
• Image display systems
• Enterprise I/O processor
• Internet access device (IAD)
• Disk controller for RAID systems
• Copier/printer board control
Technical Specifications

G2 Processor Core
- High-performance, superscalar processor core
- Floating point unit, integer, load/store, system register and branch processing unit
- 16 KB instruction cache, 16 KB data cache
- Lockable portion of L1 cache
- Dynamic power management
- Software-compatible with the Freescale processor families implementing Power Architecture technology

Power Architecture On-Chip Peripheral Logic/Memory Interface
- 133 MHz memory bus capability
- Programmable timing supporting SDRAM
- High-bandwidth bus (32-bit/64-bit data bus) to DRAM
- Supports one to eight banks of 16-, 64-, 128-, 256- or 512-bit SDRAM
- Supports 1 MB to 2 GB DRAM memory
- Contiguous memory mapping
- 272 MB of ROM space
- 8-, 16-, 32- or 64-bit ROM
- Supports bus-width writes to flash

32-bit PCI Interface Operating Up to 66 MHz
- PCI 2.2V compatible
- PCI 5.0V tolerant
- Support for PCI-locked accesses to memory
- Support for accesses to all PCI address spaces
- Selectable big- or little-endian operation
- Store gathering of processor-to-PCI writes and PCI-to-memory writes
- Memory prefetching of PCI read accesses
- Parity support (selectable)
- Selectable hardware-enforced coherency
- PCI bus arbitration unit (five request/grant pairs)

Typical Power Dissipation (est.)
- 1.8 watts @ 266 MHz (with FPU on and @ 1.8V)

Package
- 357 PBGA

Process
- 0.25μm SLM CMOS

Voltage
- 3.3V I/O, 1.8V internal

Dhrystone (2.1) MIPS
- 488 @ 266 MHz

603e Processor Core Functional Units
- Integer, floating point unit, branch processing, load/store, PCI, DMA, memory control

Peripheral Logic Functional Units
- I/O, I²C, EPIC, ATU, PCI and memory clocks, ECC controller x2 DUART

Learn More:
For current information about Freescale products and documentation, please visit www.freescale.com.