

MPC8314E Processor Family

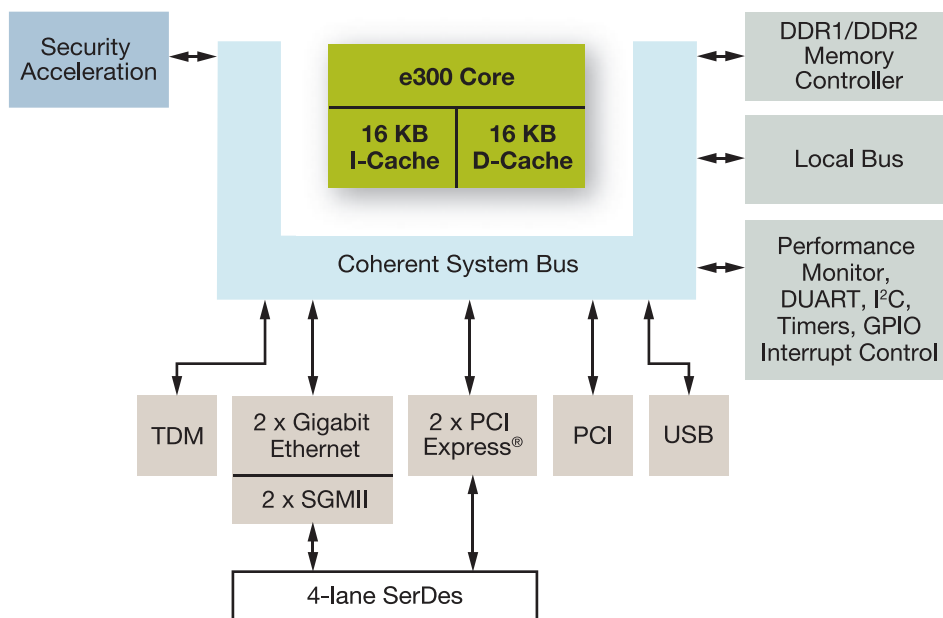
Overview

The MPC8314E communications processor, a member of the MPC8315E family, enables feature-rich consumer applications that make the digital home experience easier, richer and safer. The cost-effective MPC8314E processor meets the requirements of several small office/home office (SOHO) applications, including residential gateway, WLAN access point, printing, IP services and industrial control. It provides more CPU performance, additional functionality and faster interfaces while addressing important time to market, price, power consumption and real estate board requirements. The integration of PCI Express® Gigabit Ethernet (SGMII), High-Speed USB 2.0, TDM and low-power management makes it unique in the market place. For extremely precise clock synchronization for applications such as time-sensitive telecommunications services, industrial network switches, powerline networks and test/measurement devices, the MPC8314E features integrated IEEE® 1588 time synchronization, the leading standard.

Core Complex

The MPC8314E processor incorporates a unique configuration of the e300 (603e based) core. This configuration has been designed to include dual integer units as well as a modified multiply instruction. These architectural enhancements enable more efficient operations to be executed in parallel, resulting in a significant performance improvement. The e300 core complex also includes 16 KB of L1 instruction and data caches and on-chip memory management units (MMUs).

MPC8314E Block Diagram



■ Core ■ Accelerators ■ I/O

Features

- Functional Requirements
 - e300 core from 266 to 333 MHz with 16K D/I L1 cache
 - Second ALU for two channel voice support
- I/O Description
 - 16-/32-bit DDR1/2 266 MHz
 - Local Bus
 - PCI 2.3, 32-bit up to 66 MHz
 - USB 2.0 (host/device with PHY)
 - 2 x 1 PCI Express v1.0a
 - Two 10/100/1000 enhanced Ethernet MACs
 - RGMII, RTBI, RMII, MII, SGMII muxed with PCI Express
 - Multi-channel DMA controller
- Security Processing Unit
 - AES, PKEU, DES, 3DES, MDEU
 - Optimized for IPSEC and DTCP-IP
- Legacy Protocol Support
 - TDM—to connect to CODEC
- General Sampling: Now
- Production: Q2 2008
 - PBGA package

	MPC8315E	MPC8314E
Core	e300	e300
CPU Speed	Up to 400 MHz	Up to 400 MHz
L1 I/D Cache	16K I Cache/16K D Cache	16K I Cache/16K D Cache
Memory Controller	16/32-bit DDR/2 up to 266 MHz	16/32-bit DDR/2 up to 266 MHz
Local bus	16-bit w/NAND boot support	16-bit w/NAND boot support
PCI	32-bit up to 66 MHz (2.3)	32-bit up to 66 MHz (2.3)
PCI Express®	2x1	2x1
SATA	2 x 1 SATA 2.0 w/PHY	-
Ethernet	Two 10/100/1000 RGMII, (R)MII, RTBI, SGMII	Two 10/100/1000 RGMII, (R)MII, RTBI, SGMII
USB	One 2.0 Host or Device w/PHY	One 2.0 Host or Device w/PHY
Security	E version only	E version only
UART	Dual	Dual
I ² C	Single	Single
SPI	Yes	Yes
Interrupt Controller	Yes	Yes
Package	PBGA	PBGA
General Samples	Q4 2007	Q4 2007
Production	Q2 2008	Q2 2008

Peripheral Interfaces

The MPC8314E processor also includes a 32-bit double data rate (DDR1/DDR2) memory controller, a 32-bit peripheral component interconnect (PCI) controller, a 16-bit local bus and four direct memory access (DMA) channels.

Hardware Security Engine

The security engine (SEC 2.2) on the MPC8314E allows CPU-intensive cryptographic operations to be off-loaded from the main CPU core. The security processing accelerator provides hardware acceleration for the DES, 3DES, Advanced Encryption Standard (AES), Secure Hash Algorithm (SHA)-1 and MD-5 algorithms.

Low Cost Evaluation Board

MPC8315E-RDB (evaluation board) is available to general customers for \$499 MSRP. The kit includes Linux 2.6 BSP with optimized drivers to support all peripherals, and 6-month CodeWarrior® development tools evaluation license.

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